A shared compilation stack for distributed-memory parallelism in stencil DSLs

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Abstract

Domain Specific Languages (DSLs) increase programmer productivity and provide high performance. Their targeted abstractions allow scientists to express problems at a high level, providing rich details that optimizing compilers can exploit to target current- and next-generation supercomputers. The convenience and performance of DSLs come with significant development and maintenance costs. The siloed design of DSL compilers and the resulting inability to benefit from shared infrastructure cause uncertainties around longevity and the adoption of DSLs at scale. By tailoring the broadly-adopted MLIR compiler framework to HPC, we bring the same synergies that the machine learning community already exploits across their DSLs (e.g. Tensorflow, PyTorch) to the finite-difference stencil HPC community. We introduce new HPC-specific abstractions for message passing targeting distributed stencil computations. We demonstrate the sharing of common components across three distinct HPC stencil-DSL compilers: Devito, PSyclone, and the Open Earth Compiler, showing that our framework generates high-performance executables based upon a shared compiler ecosystem.

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1 Introduction

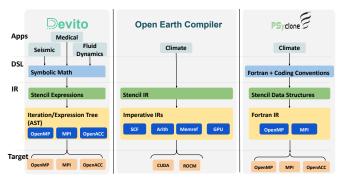
Most DSLs are purposefully designed for specific problem domains, providing focused and specialized language constructs tailored to those domains. They capture concepts for a specific domain, yet a large portion of their code base is dedicated to reasoning about generic concepts in HPC. These include the generation of directives for shared-memory parallelism, message-passing communications for distributedmemory parallelism, vectorization, arithmetic (factorization, sub-expression elimination), and loop optimizations (blocking, fusion, fission). These general-purpose optimizations are often combined with domain-specific ones. After lowering away domain-specific knowledge, compiling an intermediate representation (IR) to executable code often requires the DSL library developers to implement standard compiler passes. Sharing the developed technology between distinct projects is challenging due to integration issues with different programming languages, lack of standardization, and maintenance support.

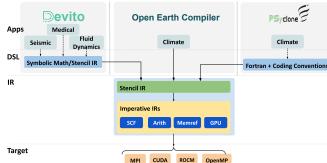
MLIR [Lattner et al. 2021] has partially solved this interoperability problem, especially for deep-learning libraries, by providing an extensible and community-driven unified IR. However, efforts are still needed to bridge the gap between HPC concepts and MLIR. This work aims to address this gap

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(a) Devito, the Open Earth Compiler (OEC), and PSyclone independently maintain abstractions for stencils and use similar imperative constructs. However, HPC features such as parallelism with MPI (in OEC) and GPUs (in PSyclone) are not universal.

(b) We combine the optimization and code generation pipelines of Devito, the Open Earth Compiler, and PSyclone. As a result, optimization passes can be shared and advanced HPC features are available to all tools.

Figure 1. Our work enables reuse of HPC and target-specific abstractions across DSL and compiler frameworks and consequently offers synergies across DSL communities, while maintaining the community-tailored interfaces of each DSL compiler.

by introducing key HPC abstractions designed for interoperability with existing MLIR dialects. We utilize xDSL [Fehr et al. 2023], a Python-native clone of the MLIR toolchain to achieve this goal. In this work we focus on explicit finite-difference (FD) stencil computations on structured grids. While FD stencils serve as a meaningful and illustrative example to showcase the applicability of the proposed techniques, the intention is to contribute to the advancement of HPC practices more broadly, with the FD stencil computation acting as a representative case study within a larger ecosystem of potential applications. This paper makes the following contributions:

- A set of HPC-specific compilation components comprising SSA dialects and lowerings between them:
 - An SSA dialect to facilitate automated domain decomposition for distributed-memory execution of stencil kernels via message-passing (section 4.2).
 - An SSA dialect for message passing as a set of modular operations in a standardized SSA-based IR (section 4.3);
- A prototype implementation of abstraction-sharing compilation stack for two HPC stencil-DSL compilers, PSyclone and Devito, based on the concepts of *SSA* and *Region*, utilizing the MLIR and xDSL compiler frameworks and extending concepts from the Open Earth Compiler (section 5).
- A performance evaluation demonstrating that our approach offers competitive performance for a range of FD stencil computations, compared to the existing domain-specific compiler stacks, for CPU shared-and distributed-memory parallelism, GPUs and FP-GAs running at scale on the ARCHER2 and Cirrus supercomputers (section 6).

The paper is organized as follows: section 2 discusses our compiler-centric approach, section 3 introduces MLIR for abstraction sharing, section 4 presents our SSA dialect abstractions that are the main contributions of this work, section 5 presents a prototype implementation for the stencil DSLs used in this work to validate our contributions, and section 6 evaluates the performance of our final software stack. Sections 7 and 8 refer to related work and conclude with future directions.

2 Stencil DSLs with Shared Abstractions

We propose a compiler-centric approach where stencil DSLs maximize the sharing of their implementation (e.g. common abstractions from their application domains or commonly used HPC abstractions) while maintaining the community-tailored interfaces and workflows that have proven critical to communicate effectively with their domain experts. By compiler-centric we mean that we build and contribute compiler infrastructure and leverage capabilities and optimizations provided by compilation frameworks, such as transformation passes, abstractions, performance optimizations, portability, and productivity.

We focus on three DSLs targetting explicit FD stencils on structured meshes, Devito [Luporini et al. 2020], the Open Earth Compiler [Gysi et al. 2021], and PSyclone [Adams et al. 2019].

FD-stencils computation pattern is an iterative computation update of an element in an n-dimensional spatial grid at time t as a function of neighboring grid elements (space dependencies) at previous timesteps $t-1,\ldots,t-k$ (time dependencies). Figure 2 illustrates a 1D-3pt Jaocobi stencil and its flow dependences. Each point is updated using values from the previous timestep and the right and left neighbors. Arrows illustrate the flow dependencies. Halo points (grey)

are read-only and extend the computational domain by the size of the stencil radius.

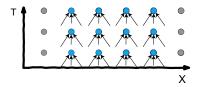


Figure 2. A 1D-3pt Jacobi stencil. Point updates depend on neighbouring values of the previous timestep

All the prementioned DSLs and their compiler implementations are developed as siloed, standalone frameworks with zero code sharing (fig. 1a). However, despite this lack of code sharing, all three stencil compilers use similar concepts and transformations for domain-specific and general-purpose HPC optimizations. To address this lack of code sharing, we propose a novel shared compilation stack for these three frameworks (fig. 1b), where domain-specific optimizations and HPC concepts are shared. User interfaces differ, but the underlying computational abstractions reason about common concepts.

Devito offers a DSL and compiler framework to automate the FD method and is primarily used in seismic inversion and medical imaging. The Open Earth Compiler was built for weather and climate models using stencils. Finally, PSyclone is designed for weather, climate, and ocean models. Devito is an embedded DSL and compiler framework written in Python. The Open Earth compiler is a domain-specific compiler offering a frontend at the stencil specification level, and PSyclone uses Fortran, augmented with specific coding conventions to connect with the HPC community.

Nevertheless, all three frameworks eventually arrive at the domain-specific concept of stencil computations. Stencil kernels (and sequences thereof) are optimized and translated into imperative code that runs on HPC machines. Hence, both the domain-specific optimization at the stencil level and the code generation for an HPC machine are conceptually similar.

We show that these similarities can be exploited to reuse and share the lower-level compilation flow across the three frameworks. The key to enabling such reuse is to share abstractions across the stencil DSL compilers. The compiler community has embraced the concepts of static single assignment (SSA) and nested control flow regions as recommended program expression and transformation approaches. The MLIR project [Lattner et al. 2021] has recently demonstrated that these concepts can be instantiated for different domains (see section 3) and used to provide a principled way to exchange information through different stages of the compilation pipeline. We embrace these concepts to design a shared compilation flow (fig. 1b) that connects these three

stencil DSL compilers. Specifically, we demonstrate that all three compilers can use a common stencil abstraction to optimize and generate code for their stencil kernels. Starting from this stencil-level abstraction (which is generated from disparate, domain-specific inputs), the shared infrastructure translates the common stencil abstractions to stencil kernels and leverages established SSA-based compiler IRs for loops, arithmetic, and memory operations. For building a stencillevel abstraction we adopt the stencil and GPU IRs in the form of MLIR dialects¹. These two dialects, introduced in Gysi et al. [2021], are discussed in detail in section 4 where we expand their features to better support the stencil DSLs studied here. This was selected as a least-friction way to lower stencil-related concepts to MLIR and LLVM. The Open Earth Compiler [Gysi et al. 2021] has already successfully targeted the lowering of stencil concepts to the MLIR framework. We reuse and extend its infrastructure, and more specifically, its Stencil IR (fig. 1a), used as the basis for the stencil dialect in this work (refer to section 4.1 for more details).

This lowering process involves a series of passes across SSA-based compiler IRs. Additionally, we introduce new IRs based on the SSA+Regions abstraction (section 3) for lowering the *stencil* dialect IR to distributed memory parallelism via the Message Passing Interface (MPI) standard. The result is a comprehensive lowering stack that automatically generates shared- and distributed-memory and GPU-accelerated computations for Devito, the Open Earth Compiler, and PSyclone.

3 Sharing Abstractions through IRs

The abstractions transformed by compilers must concretely be realized in code as some IR. IRs that maintain SSA form [Cytron et al. 1991] have proven particularly useful as their direct encoding of a program's data flow allows transformations without requiring complex analyses. Recently, the MLIR project [Lattner et al. 2021] demonstrated that adding hierarchical structure to SSA-based IRs via nested regions facilitates the modeling of higher-level domain-specific constructs, enabling development of compilers in deep learning [Abadi et al. 2015, 2016; Paszke et al. 2019], fully-homomorphic encryption [Govindarajan and Moses 2020], and hardware design [Eldridge et al. 2021; Majumder and Bondhugula 2024]. This SSA+Regions concept provides a principled way to interface distinct domain-specific IRs, which we adopt as a foundational principle in our compiler stack.

In our SSA-based IRs, the primary constructs are *operations*, chained by the *values* they define and use. Each operation in an SSA-based IR has a name, a list of values it uses called *operands*, and may define zero or more values called *results*. All values have a name, and following the SSA property, each name can be assigned at most once at any

¹https://mlir.llvm.org/docs/Dialects/

program location. We model SSA-based IRs using MLIR syntax, both for familiarity and to simplify interoperability with the existing MLIR ecosystem. For example, an addition operation (arith.add) naturally takes two operands and returns one value. Operations may also carry *attributes* that encode static information on the operation directly. For instance, the arith.constant operation carries a value attribute, corresponding to the constant value it returns. Here is an example in MLIR syntax (producing the integer value 84 in %res):

```
%0 = "arith.constant"() {value = 42: i32} : () -> (i32)
%2 %res = "arith.add"(%0, %0) : (i32, i32) -> (i32)
```

Each value has an associated *type*, such as the 32-bit integer type i32 used in the example. For readability, we sometimes shorten the syntax of operations by omitting the parentheses, the attribute names, or the redundant types. This results in the shortened syntax %0 = arith.constant 42: i32 for the constant operation.

To represent control flow and to model higher-level abstractions, operations can be nested in *regions*, which are themselves attached to operations. A region contains a control-flow graph of *blocks*, each containing both a list of values (the *block arguments*) and a list of operations. Since the abstractions we introduce in this paper only use regions with a single block, we will omit the notion of *blocks* for the rest of the paper, and will use the term *region arguments* to refer to the region arguments of the first (single) block in a region. As an example of the structure that regions capture, a for loop can be expressed as

This loop iterates from %lo to %hi with a stride of %stride. Its body is represented as a nested region that takes the loop induction variable %i as a *region argument* and then contains a list of operations in the block's body.

Sets of operations, types, and attributes related to a common abstraction are organized into distinct units called *dialects*. For example, the add and constant operations are part of the *arith* dialect that covers arithmetic operations. On the other hand, integer attributes (42: i32) and integer types (i32) are part of the *builtin* dialect.

While various compiler frameworks use SSA-based IRs, the introduction and use of regions is more recent and central in MLIR and xDSL. MLIR is an LLVM subproject that supports SSA and regions in a performance-focused C++ compiler framework. It comes with pre-defined abstractions for arithmetic, structured control flow, memory references, GPUs, and many more. The xDSL project is a Python-native

clone of MLIR that provides an embedding of SSA and regions into Python facilitating interoperability with Python-based DSLs. Similar to MLIR, xDSL is open-source and publicly available on GitHub². Both frameworks are built on the previously introduced concepts of SSA and Region and share the same textual representation to share infrastructure without tight coupling of code. Users may introduce their own abstractions by defining new dialects specific to their application domain. Since most DSLs we are targeting are written in Python, we start our compilation pipeline from xDSL and define our custom abstractions there. We develop dialect-specific lowerings from xDSL to existing MLIR dialects and then hand off to the MLIR toolchain where we apply further lowerings to target particular hardware.

4 SSA Compiler Abstractions for HPC

The memory requirements of computational science problems in HPC often exceed the capacity of DRAM on a single platform. Fortunately, many HPC problems lend themselves to spatial domain decomposition, allowing for the distribution of computational tasks across multiple compute nodes within a cluster. Thus, domain decomposition and messagepassing abstractions are considered integral parts of HPC.

While MLIR provides several dialects that also benefit HPC users, such as *omp* for OpenMP shared-memory parallelism (SMP), *gpu* for generic GPU programming across NVIDIA and AMD GPUs, and *vector* for vectorizing computations, it does not provide a means to control distributed memory parallelism (DMP).

We extend the capabilities of the *stencil* dialect introduced in Gysi et al. [2021] to target multi-node HPC clusters through a novel, extended version of this dialect (section 4.1). This dialect captures the geometric decomposition pattern of where the domain is decomposed into rank-local domains. The rank-local domains communicate at predefined points in the computation. One of the uses of the *dmp* dialect is in the developed lowerings from the existing *stencil* dialect. While the *stencil* dialect contains the mathematical abstract representation of the problem, the *dmp* carries a more concrete realization. Although still at a fairly high level from a parallelism perspective, we consequently lower to the *mpi* dialect, an even lower-level realization of the parallelism and decomposition.

Frameworks can represent their stencil computations using the *stencil* dialect, benefiting from common IR and semantics. The *dmp* dialect is an abstraction for distributed-memory parallel (DMP) operations, such as data exchanges through message passing (section 4.2). Through the *dmp* dialect, frameworks that have expressed their IR in *stencil* benefit from automatically decomposing and distributing the computational domain to the MPI ranks that are used for the computation. We refer to the data owned by an MPI

²https://github.com/xdslproject/xdsl

rank as "rank-local" data. Finally, we introduce an MPI-based dialect (section 4.3) that mirrors MPI's point-to-point and collective communications and serves as a lowering target for the *dmp* dialect. Communications are expressed using this novel dialect, facilitating the development of codes leveraging message passing. The implementation of *stencil*, *dmp*, and *mpi* dialects is open-source and available online.

4.1 A Stencil Dialect

The initial implementation of the *stencil* dialect was introduced as part of the Open Earth compiler [Gysi et al. 2021], to represent stencil computations and their sequences by capturing essential information, including iteration space bounds and stencil update patterns. This dialect acts as an intermediate step, helping to close the semantic gap between the scientist's problem description and the concrete implementation on CPUs and GPUs.

A major benefit of the *stencil* dialect is that it is problem, domain, and hardware independent, in contrast, for instance, to other approaches such as Essadki et al. [2023] and Li et al. [2024]. For example, Essadki et al. [2023] introduced a cfd MLIR dialect for stencils associated with Computational Fluid Dynamics (CFD) problems, with operations and transformations focused on this specific problem. Consequently, their dialect is tied to one class of DSL rather than providing the ability to generalize across domains. By contrast, the work described in Li et al. [2024] targets the porting of stencil applications to the Sunway SW26010 heterogeneous manycore processor, with the dialect containing operations influenced by the target machine architecture. Instead, when using the stencil dialect from Gysi et al. [2021], a programmer's code is lowered to a general-purpose description of a stencil computation independent of the hardware architectures. A major contribution of Gysi et al. [2021] was to demonstrate that this general description of a stencil computation contains enough information for subsequent transformations to effectively operate upon when generating optimized HPC target executables.

In this work, we integrated the *stencil* dialect into the xDSL framework and extended the dialect to enable integration with our DMP and MPI abstractions, facilitating support for various lowering targets, including CPUs, GPUs, and FPGAs. Due to its general purpose nature, the *stencil* dialect contains 11 operations in total, compared, for instance, to Essadki et al. [2023], which only contains two. The following list briefly highlights the most important operations and types in the *stencil* dialect.

- stencil.field is a type that represents the memory buffer from which stencil input values will be loaded, or to which stencil output values will be stored
- stencil.temp is a type which represents stencil values and which the stencil.apply operation operates over

- stencil.access is an operation that accesses a value from a stencil.temp given the specified offset relative to the current position.
- stencil.store is an operation that writes values to a field on a user-defined range.
- stencil.load is an operation that takes a field and returns its values.
- stencil.apply is an operation that accepts a stencil function plus parameters and applies this stencil function to those parameters, generating an output stencil.temp field.
- stencil.return is an operation that terminates the stencil.apply stencil function and writes the results of the stencil operator to the temporary values returned by the stencil.apply operation.

Listing 1 provides an example of the stencil dialect to compute a 1-dimensional 3-point Jacobi calculation (see fig. 2). The stencil. load operation loads the values held in a buffer (the !field type) into a !temp type, which can be operated upon, whilst stencil. store stores the resulting values back to a buffer. It was found in Gysi et al. [2021] that working with value semantics enables powerful optimization across stencil operators, and whilst those are not demonstrated in this work, we purposefully keep this design to ease their integration in further work. The stencil.apply operation defines the Jacobi stencil computation, which is applied to values passed as operands. Its region represents the computation of individual outputs and runs across the entire field, where stencil.access accesses input values with a relative offset to the current index. For instance, in listing 1, the direct grid neighbors and the value itself are accessed. The stencil return operation then returns the result for the current grid cell.

Working with authors of the *stencil* dialect, we have made various enhancements. For instance, in the original dialect, bounds information was encoded as attributes of MLIR operations. However, this required additional analysis and transformations in lowering from the logical coordinates of the

Listing 1. Example MLIR for 1-dimensional 3-point Jacobi stencil.

stencil representation to zero-based memory operation indexing. To avoid these complexities, we modified the dialect to associate domain bounds information with the values themselves through their types. This allows any operation using stencil-related types to access this information directly through their operands. It not only simplifies the existing stencil transformations but enables independent lowering to the DMP abstraction, decoupling this from stencil-specific operations that define logical coordinates.

Previously, the *stencil* dialect was only capable of representing 3D stencils and we have also enhanced the dialect so that it can be used with stencils of any number of dimensions. Not only does this enable us to run simpler, 1D and 2D problems, but furthermore provides flexibility for more complicated future domains. The original dialect was specifically tailored to target GPUs and-so we have enhanced the stencil transformations by providing an additional lowering pipeline which is better suited for shared memory parallelism by leveraging loop tiling to improve data locality.

By incorporating these enhancements, we improved the *stencil* dialect's compatibility with other MLIR dialects, and specifically based upon requirements from other contributed dialects in this section. For instance, it is possible for subsequent transforms to determine the minimal halo shape and size that is required for distributed memory by scanning the stencil. access offsets which operate used on inputs of a stencil.apply. Such information can then be used as a basis for automatically distributing the computation on multiple nodes.

Limitations. The main functional limitation of the stencil dialect is the requirement for compile-time known bounds. Whilst this requires recompilation of code when the problem sizes changes, the performance benefits delivered by having this information statically available during compilation are significant. For example, known bounds enable constant-folding of most of the memory access address computations and thus reduce register pressure which is critical to increasing parallelism on GPUs. Due to the nature of DSL compilers, propagating bounds from the call site to the stencil expression is usually not difficult in practice, while the existence of compile-time known bounds greatly aids in implementing more complex compiler analysis and optimization passes.

Another limitation is the absence of a high-level representation for modeling boundary conditions, and this feature is scheduled for future work. The current version of the dialect is flexible enough to manually encode boundary conditions as conditionals over the memory accesses. However, expressing these at a higher level could lead to more opportunities for optimizing code generation and enhancing the supported use cases for the users.

4.2 dmp dialect: An IR for Domain Decomposition

This section introduces a novel dialect for distributed memory parallelism (DMP), the *dmp* dialect. *dmp* is used to express parallel communication patterns as modular building blocks that lower computational dialects, such as *stencil* to an IR for DMP. *dmp* offers a mechanism for describing the exchange of rectangular subsections of data among nodes. Additionally, we introduce a pass to convert a stencil kernel into an IR for distributed computations. This pass allows for optimizing intra- and inter-node performance gains using the *dmp* dialect for targeting large-scale runs.

The contributed *dmp* dialect expresses this communication pattern using the dmp. swap operation (listing 2), which takes a memref as an argument and has attributes that specify which subsections should be exchanged with which ranks. The swap is configured using two parameters, the number

Listing 2. A high-level declarative expression of a data subsection exchange from some buffer.

and the cartesian topology of the ranks participating in the swap (using the dmp. grid attribute) and a list of exchanges that are to be carried out (using the dmp. exchange attribute). As illustrated in fig. 3, each exchange marks two rectangular subsections of the memory region to exchange (one to send from, one to receive into) and the relative offset of the rank with which these regions are to be exchanged.

While *dmp* operations could be inserted by the frontend framework as desired, we offer a shared pass that automatically prepares stencil programs for distributed execution. This pass is parameterized by information on the topology of MPI ranks in the computation, along with a decomposition strategy. This strategy describes how the data should be distributed among nodes. Given this information, we equally decompose the domain represented in stencil to a "local" data domain, to the available ranks. The stencil dialect is also responsible for adding the necessary halos to local domains. Subsequently, dmp. swap operations are inserted before each load, ensuring that neighboring ranks hold the updated data before proceeding to the following stencil computation. While this may generate redundant data exchanges, a subsequent pass eliminates them via a further pass analyzing the SSA data flow. Figure 4 illustrates the lowering of the IR and the resulting stencil domain.

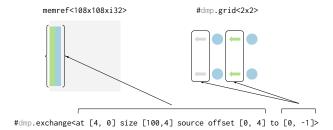


Figure 3. The exchange declaration defines a rectangular region of size 100 by 4, starting at (4, 0) inside a memref that needs to be updated with data from the neighbor at the relative position (0, -1). In exchange for receiving this data, a rectangular region of the same size, but offset by (0, 4) will be sent to the neighbor. This allows us to effectively model halo exchanges in a declarative way.

Internally, a *decomposition strategy* is represented by a class that exposes an interface that allows a rewrite pass to calculate the local domain from the global domain. It also provides the rank layout (the dmp.grid attribute) and generates the halo exchange declarations (the dmp.exchange attributes) from the stencil access patterns. This extensible design allows adopters to supplement our default slicing strategy with their own optimized versions if they require more exotic exchange patterns. We provide a standard slicing strategy that supports 1D, 2D, and 3D decomposition.

The design of the *dmp* dialect is directly influenced by design choices made in the *stencil* dialect. The compile-time known bounds of the stencil expression greatly aided in reducing the complexity of the *dmp* operations and transformations, demonstrating that the simplicity of the *stencil* dialect directly benefits the available compiler optimizations.

Limitations. The *dmp* dialect is a prototype implementation of domain decompositions for stencil computations. It is designed to operate on contiguous, hyper-rectangular subsections of the domain and, therefore, does not support operations on sparse or non-rectangular-shaped domains. Extending the dialect to cover more data layouts is projected for future work.

Another limitation arises due to the fact that one exchange operation corresponds to one halo exchange, making the implementation of optimizations such as communication-computation overlap and exchanging multiple halos simultaneously more complicated than it needs to be. Finding a suitable extension to the *dmp* dialect for more application domains and more efficient rewrites is also projected as an interesting direction for future work.

4.3 mpi dialect: An IR for Message Passing

Our final contribution to the MLIR ecosystem is the *MPI* dialect, designed to mirror MPI's point-to-point and collective communications. The *mpi* dialect has already been upstreamed to the MLIR compiler toolchain³. This dialect serves as a target for our *dmp* dialect and is lowered to MPI library function calls.

Our work here comprises the dialect itself, containing the abstract operations and types. The operations correspond to the MPI calls, while the types represent MPI types such as request handles, communicators, and data types. Additionally, we have introduced operations to reduce the friction between the MPI and the MLIR ecosystems. These operations enable the expression of common MPI concepts outside of the library calls, such as request object lists and interactions with memory references. Because MLIR and the LLVM backends lack an intrinsic notion of MPI, we have also developed a lowering that will convert the MPI dialect into the underlying function calls and associated memory allocations using the low-level *llvm* and *func* MLIR dialects. The contributed *mpi* dialect currently supports the following subset of the MPI 1.0 standard operations:

- Blocking and Non-blocking Point-to-Point communications: MPI_Send, MPI_Recv, MPI_Isend, MPI_Irecv
- Nonblocking request operations: MPI_Test, MPI_Wait and MPI_Waitall
- Blocking reductions: MPI_Reduce and MPI_Allreduce
- Broadcast and Gather collective: MPI_Bcast, MPI_Gather
- Process Management: MPI_Init, MPI_Finalize, MPI_Comm_rank and MPI_Comm_size

While this subset of MPI operations provides the necessary building blocks for the current needs of our MPI applications, the design allows for extensions. Additionally, we provide operations that simplify targeting *mpi* from higher levels of abstraction. Our compiler transformations and lowerings leverage these operations to implement DMP.

One of the lowerings we provide transforms *dmp* to *mpi* operations. Note that there is nothing MPI-specific in the *dmp* dialect, allowing targeting other communication libraries if desired. Lowering to *mpi* involves several steps, including allocating temporary buffers, building the MPI exchange mapping, packing/unpacking data to/from buffers, and issuing non-blocking send/receive calls. Figure 4 shows the resulting transformation, with some details omitted for readability, such as setting skipped request objects to the null request and temporary send/receive buffer allocations and

³https://mlir.llvm.org/docs/Dialects/MPI/

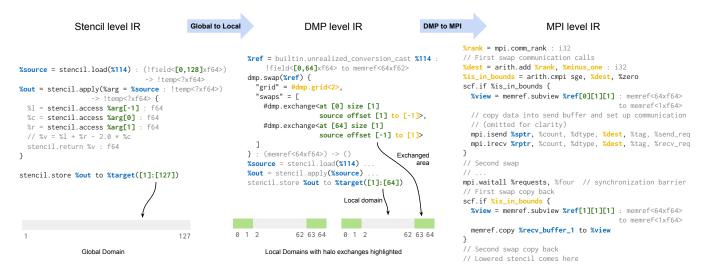


Figure 4. A global stencil being transformed to a local *stencil* + *dmp*, and then lowered to MPI. We highlight the data being operated on, shape and halo information, and communication-related information. This showcases how we can enrich the IR with relevant information to perform efficient rewrites at every level of abstraction.

de-allocations. Since MPI communication often happens inside loops, any loop invariant calls are hoisted as part of this transformation.

As LLVM has no concept of MPI, we lower these operations to regular function calls using the *func* dialect. Motivated by the distribution on our target platform (ARCHER2), we support the *mpich* implementation of the MPI standard. To make use of MPI, it is usually required to include the implementations C header file, a notion not supported by MLIR. Instead, we extract magic values from our library's header file and substitute them for e.g. datatype constants during the lowering process. This makes our provided MPI lowering specific to the *mpich* library, but this strategy can be adapted to other MPI libraries like OpenMPI. Futhermore, there is an ongoing effort to provide one standard MPI ABI, greatly simplifying this problem [Hammond et al. 2023].

Listing 3 illustrates the operation mpi . send for sending a memref containing 128 double-precision floats. In line 1, an operation in the MPI dialect is employed to unwrap a memref into an LLVM pointer to the underlying buffer %buff, the number of elements in the buffer %count, and the corresponding MPI datatype. IR similar to the one in listing 3 is generated by our lowering pass from *dmp* to *mpi*, except using non-blocking communication.

As described, our *mpi* dialect must be lowered to function calls that can be effectively compiled by LLVM. The lowered version of listing 3 is sketched in listing 4. In lines 1–6 of listing 4, it can be seen that the mpi .unwrap_memref operation has been expanded to extract a pointer to a contiguous memory area. Furthermore, since the size of the memref is compile-time known, the %count can be statically calculated as well. The MPI datatype constant here is specific

```
%buff, %count, %dtype = mpi.unwrap_memref(%memref)
: (memref<64x2xf64>) -> (!llvm.ptr, i32, !mpi.datatype)
mpi.send(%buff, %count, %dtype, %dest, %tag)
: (!llvm.ptr, i32, !mpi.datatype, i32, i32) -> ()
```

Listing 3. The *mpi* dialect makes it easy to target distributed memory systems from higher levels of abstraction by providing interfaces to work either with raw pointers or memrefs. Here we show a basic MPI_Send call of an MLIR memref.

Listing 4. The *mpi* dialect provides a uniform layer for higher-level dialects to target, which are then lowered to implementation-specific function calls and constants.

to the MPI library and was extracted from a C header file. It is worth noting that switching to a different underlying MPI implementation would require a modification to this part of the lowering process. The mpi. send is replaced with func.call, an operation in the standard *func* dialect that issues a function call. In line 11, an external function definition of the MPI_Send function, is appended to the end of the MLIR module.

5 Lowering stencil DSLs to MLIR

This section briefly introduces the frameworks used and then details the methodology to leverage the synergies exploited from the contributed shared infrastructure. Figure 1b schematically presented the shared infrastructure contributed by this work. Devito and PSyclone lower their IRs to the *stencil*, *dmp* and *mpi* dialects, benefiting from the advantages presented in section 4. Additionally, they leverage "out-of-the-box" lowerings to other dialects optimized for HPC, such as *omp*, *gpu* designed for parallel execution on CPUs and GPUs.

5.1 Devito

Devito [Louboutin et al. 2019; Luporini et al. 2020] is an opensource Python DSL and compiler framework widely used in academia and industry, aiming to ease the development of HPC finite-difference PDE solvers. Devito's symbolic DSL is based on Sympy [Meurer et al. 2017], facilitating expressing and solving PDE simulations. Devito's compiler framework automates the conversion into optimized FD kernels for efficient execution on CPUs and GPUs. An example of the Devito DSL for modeling a 2D heat diffusion problem is shown in listing 5.

```
# Model the problem and automatically generate code
grid = Grid(shape=(126,))
u = TimeFunction(name='u', grid=grid, space_order=2)
eqn = Eq(u.dt, 0.5 * u.laplace)
op = Operator(Eq(u.forward, solve(eqn, u.forward)))
# JIT-compile the code and run
op(t=timesteps)
```

Listing 5. The high-level symbolic code to model 1-dimensional heat diffusion in Devito DSL. Users can only focus on modelling, all machinery for optimized HPC code generation is abstracted away.

Devito's separation of concerns is benefiting interdisciplinary research and development by reducing time-consuming and error-prone practices widely encountered in stencil codes. Devito uses a high-level symbolic mathematic-textbook-like abstraction as input that is very close to what mathematicians, physicists and geoscientists are familiar with. It assists interdisciplinary scientists with the rapid development of simulation codes for wave propagators or other PDEdominated problems, as it facilitates the development of mathematically sophisticated PDE simulations, the implementation of stencil kernel adjoints, boundary conditions, sparse non-aligned-to-the-structured-grid operations [Bisbas et al. 2021] and others. All the compiler optimizations are abstracted away from the DSL user: arithmetic and loop performance optimizations (e.g., common sub-expression elimination, loop tiling, factorization), and backend-specific optimizations, such as SIMD vectorization, SMP and DMP, and GPUs. Devito's compiler automates optimization passes,

allowing users to apply further tuning heuristically. On completion of the compiler passes, high-performing C code for efficient PDE solvers is automatically generated.

The shared Devito-PSyclone approach to lowering stencil IRs to xDSL is shown in fig. 6. The upper part of the fig. 6 illustrates an overview of lowering Devito's stencil representation to xDSL and, subsequently, MLIR and LLVM. Initially, Devito's symbolic input undergoes lowering to a representation, which encapsulates the FD-stencil representation regarding iteration spaces, memory accesses, mathematical operations, and many more.

The primary Devito object that contains the necessary semantics in Devito is a group of expressions. Subsequently, these are parsed and lowered to stencil expressions (fig. 5). Building upon the example presented in listing 5, fig. 5 shows some of the IR that Devito is using to represent mathematical equations. We parse info on read and write accesses from Devito's IR, and use this information to construct expressions using the *stencil* dialect, which will then be further lowered as described in fig. 4.

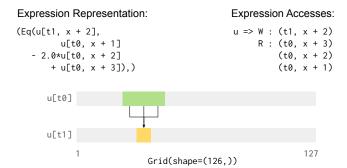


Figure 5. Extracting Devito's IR lets us generate stencil dialect expressions. Devito provides info on read and write accesses (refer to fig. 4).

While a number of dialects are used when lowering Devito to the xDSL representation (refer to fig. 6), some of the main corresponding matches involved while visiting Devito structures are: the translation of mathematical expressions using operations from the *func* and *arith*, translation of Devito's memory accesses to *memref* and *stencil* dialect, translation of the problem dimensions to structured control flow using the *scf* dialect and targetting specific backends using the *mpi* and *gpu* dialects. The integration with Devito happens at the highest possible level of Devito's compiler IRs to evaluate the optimization capabilities MLIR offers compared to the main Devito optimization pipeline. This approach helps to compare pipelines that do not share any optimizations and start from the same level of abstraction.

The contributed *stencil* dialect facilitates the lowering from Devito to build the FD structured grid, the necessary ghost-cell read-only region, the stencil coefficients, and memory accesses. Subsequently, we add the temporal and spatial

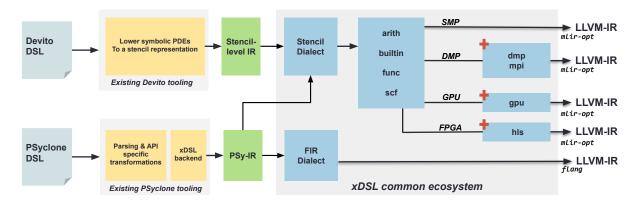


Figure 6. An overview of the Devito and PSyclone xDSL integration. The existing Devito IR (green) is lowered to xDSL's *stencil* dialect, whereas an xDSL backend for PSyclone has been written and integrated into the existing tooling, which generates a bespoke PSy-IR matching PSyclone's own IR. Irrespective, both progressively lower to xDSL's cloned MLIR dialects, plus the novel-contributed ones (*dmp*, *mpi*, *hls*) following the same shared path. Finally, the LLVM-IR code is generated.

loops, including time-buffering. We benefit from applying transformation and optimization passes from the shared infrastructure available from the MLIR community⁴ such as cse, loop-invariant-code-motion, fold-memref-alias-ops and convert-scf-to-openmp. Finally, HPC code leveraging SMP, DMP for CPUs, and GPUS is generated for several targets and then compiled and executed. We evaluate these variants against standalone Devito in section 6.

5.2 PSyclone

PSyclone [Adams et al. 2019] is a DSL for Fortran codes, enabling scientists to write their kernels in Fortran, a language that they are already familiar with, and then leverage a translation layer that abstracts the mechanics of the computation and parallelism. PSyclone is popular with weather and climate, for instance, the Met Office's next-generation weather model, LFric [Melvin et al. 2017], is using this technology and they are also involved in several other activities around PSyclone such as the NEMO ocean model port [Porter et al. 2018]. The major design feature of PSyclone is to enable a separation of concerns, where scientists develop the algorithm and kernel layers, both representing the mathematics of their problem and directing the sequence of maths operations that should be run, with the tool then generating the PSy layer. This PSy layer connects the algorithm and kernel and layers together, for instance, applying distributed memory parallelism. Furthermore, the PSyclone compiler will analyze the scientist's provided code and undertake optimizations and transformations, such as applying OpenMP or OpenACC at the loop level for threaded parallelism and GPU acceleration respectively.

However, the compilation stack of PSyclone is siloed with a bespoke translation layer that has been written in Python and, after parsing the Fortran source code, builds an internal intermediate representation based in a Directed Acyclical Graph (DAG) form. This IR is then operated upon by transformations bespoke to the PSyclone compiler before the IR is transformed into either Fortran or C. Domain-specific APIs enhance the core functionality of PSyclone, where an API contains a specialized set of transformations that target individual codes or scientific areas. For the results discussed in this work we leverage the NEMO API which has been developed to enable PSyclone to target the NEMO ocean model [Porter et al. 2018].

5.2.1 Lowering PSyclone to xDSL/MLIR/LLVM. Figure 6 illustrates the shared Devito-PSyclone approach for lowering abstractions to xDSL, then building upon the shared transformations, existing MLIR dialects and new HPC dialects presented in this paper. Consequently, the PSyclone DSL is now a thin abstraction layer a-top a common shared ecosystem which is also used by Devito as described in section 5.1. We still use the lexing and parsing of PSyclone to build the PSyclone IR. This is then passed directly to our PSyclone xDSL backend to generate our own *PSy IR*, an xDSL-based IR that closely resembles PSyclone's own IR. Whilst this is still heavily PSyclone dependent, as it is in DAG form, there is a rich structure to the representation that appropriate transformations can exploit and a one-to-one mapping between PSyclone's existing IR and our xDSL *PSy-IR*.

An example of such a transformation that can be applied at this stage by the PSyclone xDSL backend is the identification of stencils from Fortran loops. Any identified stencils are represented in the *PSy-IR* dialect which is then lowered to SSA form. Once in SSA form the flow is within the common xDSL ecosystem and there are two main dialects that *PSy-IR* is lowered to. The stencil dialect, with the flow exactly as described for Devito in section 5.1; and the FIR dialect, used by Flang to represent Fortran. Lowering the non-stencil aspects into this standard Fortran dialect not only means that

⁴https://mlir.llvm.org/docs/Passes/

we preserve the semantics of the surrounding code but also the *escape hatch* of PSyclone which is the ability to handle all Fortran that is not transformed by PSyclone itself.

Whilst a mix of dialects is natural when working with MLIR, this raises a challenge with the LLVM tooling because the FIR dialect is separated from other dialects. Flang, which defines the FIR dialect, is only capable of working with that dialect and a very small subset of standard dialects such as arith and func. Likewise, mlir-opt, which is used to operate on the standard dialects is unaware of FIR. These different standard dialects are crucial; for instance, the gpu dialect is required for launching on the GPU and the memref dialect for handling memory within stencils, but Flang is not able to process this.

As shown in fig. 6, the FIR and stencil aspects are kept separate, with Flang used to build the LLVM-IR from the FIR dialect and mlir-opt the lowered dialects from transformations on the stencil dialect which are wrapped in functions for each stencil. Ultimately, this generated LLVM-IR is passed to the corresponding LLVM backend for the target architecture, and compiled into object files that are linked together to form the target executable where FIR can then call into the stencil dialect components by issuing the appropriate function calls.

6 Evaluation

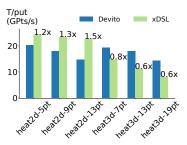
This section presents the experimental evaluation of this paper's contributions versus the standalone Devito and PSyclone compiler stacks. The systems used for the experiments were: (a) ARCHER2 HPE Cray EX Supercomputer nodes comprising a dual AMD EPYC 7742 64-core 2.25GHz processor with 128 cores. Each node has 8 NUMA regions and 16 cores per NUMA region, 32kB of L1, 512kB of L2 cache per core, 16MB L3 cache for every 4 cores and supports AVX2 vectorization. It has an HPE Slingshot interconnect with 200 Gb/s bandwidth, dragonfly topology, and nodes are organized into groups of 128. CCE's Cray Clang 11.0.4 was used. (b) Cirrus GPU compute nodes consisting of four NVIDIA Tesla V100-SXM2-16GB (Volta) GPU accelerators. On Cirrus, we used version Cray Clang 11.4.100, nvc 22.11 from NVIDIA HPC SDK 22.11, and CUDA 11.6.

We use modified versions of xDSL, PSyclone, and Devito. Experiments were executed with the Devito code available here [xdslproject/devito] and xDSL code available here [xdslproject/xdsl]. For the performance evaluation of the stencil kernels we use *GPts/s* (a.k.a *GCells/s*) for throughput.

6.1 Devito

We use two benchmarks from CFD and seismic imaging: (i) heat diffusion, a Jacobi-like stencil, and (ii) the isotropic acoustic wave equation. We benchmark both problems in 2D and 3D for varying space discretization orders (SDO) of 2, 4, and 8, resulting in 5-, 9-, 13-pt for 2D and 7-, 13-, 19pt stencils

for 3D. The isotropic acoustic wave equation uses a 2nd order accurate approximation in time, resulting in more points being read at the time dimension. On ARCHER2, the problem size is 16384² for the 2D and 1024³ for the 3D case. On Cirrus, the problem size is 8192² for the 2D and 512³ for the 3D case. The simulation time in timesteps is 1024 for the 2D and 512 for the 3D case. For the strong scaling experiments, we focus on the 3D problems with a bigger working set. For all benchmarks, we use a 32-bit single-precision floating point numbers.



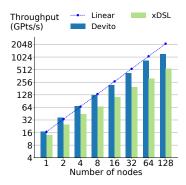
(a) Heat diffusion kernels



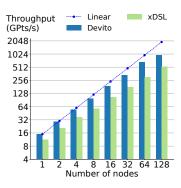
(b) Acoustic wave kernels

Figure 7. xDSL-Devito does well on lower AI kernels, mostly dominated by memory bandwidth, but does not reach performance parity with Devito for high-AI problem instances.

Figure 7 evaluates xDSL-Devito versus the native Devito. This experiment uses 8 MPI ranks and 16 OpenMP threads per rank on an AMD EPYC 7742 node of ARCHER2, to better suit the NUMA architecture of the underlying architecture. The Devito benchmark was optimized using the full suite of flop reduction, DMP, SMP, and SIMD vectorization optimizations [Bisbas et al. 2023; Luporini et al. 2020]. Devito's solvers are highly efficient, as established on roofline plots in related work [Bisbas et al. 2021; Luporini et al. 2020], ensuring we compare against a highly competitive baseline. xDSL-Devito's performance outperforms Devito for low arithmetic intensity (AI) kernels. However, Devito's flop reduction optimizations pay off for higher AI. One reason for this is the limited vectorization performance of our current lowered LLVM IR, which is essential for stencil kernels [Henretty et al. 2011].



(a) so4 Heat diffusion kernel

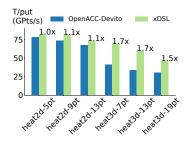


(b) so4 Acoustic wave kernel

Figure 8. xDSL-Devito's strong scaling follows the trend of Devito, but Devito still outperforms xDSL with its advanced communication techniques.

Figures 8a and 8b show the strong scaling of the heat diffusion and acoustic wave stencil kernel, respectively. We benchmark both kernels for a 3D problem and SDO of 4. We use a whole ARCHER2 group of 128 nodes scaling up to 1024 MPI ranks, totaling 16384 cores. We observe that xDSL-Devito exhibits strong scaling that may not match Devito's performance but still maintains the scaling trend. This regression is expected, as Devito supports more advanced communication techniques, consisting of 3D diagonal exchanges leading to more robust and efficient scaling. More details on the domain decomposition techniques employed by Devito can be found in Bisbas et al. [2023]. Extending computation/communication patterns in the *dmp* dialect is planned for future work. There is definitely space for more improvements on xDSL's end, which is discussed in section 8.

Figure 9 presents the GPU evaluation. We run on a V100, using OpenACC GPU offloading for Devito⁵, reporting the best performance among using *collapse(2)*, *collapse(3)* or *tile(32,4,8)* for the spatial loops of the stencil. xDSL-Devito's kernels use MLIR lowerings to CUDA [Gysi et al. 2021] and use tiled execution. These lowerings allow us to benefit from



(a) Heat diffusion kernels



(b) Acoustic wave kernels

Figure 9. xDSL's lowerings through CUDA outperform Devito's tiled OpenACC kernels for more than 1.5x when it comes for 3D kernels on an NVIDIA V100

an out of the box CUDA backend. Evaluation shows, as expected, that Devito/xDSL CUDA kernels outperform Devito's OpenACC for the higher-intensity wave kernels while being mostly on par with the rest of them. Profiling using nsys⁶, we observe that the main reason is superfluous synchronization overhead on each kernel launch, which is amortized in the larger kernels by the kernel runtime itself. The MLIR version used does not yet offer a built-in solution for this.

6.2 PSyclone

We have selected two benchmarks to explore performance for our approach with PSyclone, the first is the Piacsek and Williams advection scheme [Piacsek and Williams 1970], commonly used by Met Office codes such as the MONC highresolution atmospheric model [Brown et al. 2015], for calculating the movement of quantities through the atmosphere due to kinetic effects (e.g. wind). The second benchmark is the tracer advection kernel from the NEMO ocean model and part of the PSyclone benchmark suite [Science and Technology Facilities Council (STFC) 2021]. Both these schemes are extracted from production codes and the benchmarks are different in a couple of crucial ways. Firstly, PW advection contains three separate stencil computations across three fields, whereas tracer advection comprises 24 stencil computations across six fields. Each stencil computation involves many individual calculations, and for tracer advection, there

⁵DevitoPRO's license would be needed to compare against CUDA

⁶https://developer.nvidia.com/nsight-systems

are many more computations than fields due to dependencies between computations generating intermediate results. Furthermore, the tracer advection benchmark contains an outer loop where the entire stencil calculation is executed for 100 iterations.

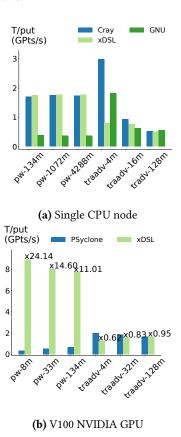


Figure 10. xDSL-PSyclone single node CPU (ARCHER2) and GPU (Cirrus) throughput, where tracer advection benchmark performance is limited by the MLIR scf parallel lowering transformations.

Figure 10a provides a performance comparison of using our approach, *xDSL-PSyclone*, against PSyclone where the target code is compiled with the Cray compiler, *Cray-PSyclone* and the GNU compiler *GNU-PSyclone*. We report throughput across our benchmarks (*pw* for PW advection and *traadv* for tracer advection) at different problem sizes. It can be seen that for the PW advection benchmarks the performance delivered by xDSL slightly exceeds that of PSyclone with the Cray compilers, whereas PSyclone with the GNU compiler is performing considerably worse. This demonstrates that the Cray compiler is undertaking numerous HPC optimizations over and above the GNU compiler, and given that xDSL is slightly outperforming the Cray compiler our stack can undertake similar levels of optimizations.

However, in fig. 10a it can be seen that the performance is different for tracer advection, where for smaller problem

Table 1. xDSL-PSyclone supports execution on an Alveo U280 FPGA, which is not supported by PSyclone and can undertake auto-tuning of the kernel to a dataflow architecture delivering significant performance improvements compared to the initial version.

Benchmark	Through _l Initial	out (GPts/s) Optimized	Performance improvement
pw-8m	1.0×10^{-3}	1.0×10^{-1}	100x
pw-33	8.5×10^{-3}	1.4×10^{-1}	165x
pw-134m	8.6×10^{-3}	1.5×10^{-1}	175x
traadv-4m	4.5×10^{-4}	5.1×10^{-2}	113x
traadv-32m	3.6×10^{-4}	7.7×10^{-2}	214x

sizes xDSL is considerably slower than PSyclone with both the Cray and GNU compilers, although the performance gap narrows for larger problems. The reason for this is the number of individual stencils, where for the PW advection benchmark the three stencil computations are fused into one single stencil region by xDSL, but with tracer advection there are 18 individual stencil regions due to dependencies. Limitations in the lowering from <code>scf.parallel</code> to the OpenMP dialect result in each stencil region being lowered by MLIR into a separate parallel region. Consequently, the <code>kmp_wait_template</code> function, which spins on a barrier waiting for parallel worker threads to complete, was the most runtime-intensive function when profiling smaller domain sizes. At larger problem sizes this issue, whilst still present, is ameliorated.

We then explored performance on a NVIDIA V100 GPU accelerator which is reported in fig. 10b. On the GPU xDSL considerably outperforms PSyclone with the NVIDIA compiler for the PW advection benchmark and this is due to how data allocation is handled. PSyclone uses the managed memory option, whereas the xDSL GPU lowering detects that explicit memory allocation on the device will be more performant and handles this directly. Consequently, when the PSyclone compiled PW advection benchmarks were executed we found that there were a large number of unified memory GPU page faults which do not occur with xDSL.

The performance pattern for tracer advection on GPUs demonstrated in fig. 10b is similar to that of a single node illustrated in fig. 10a, where xDSL lags PSyclone, especially for smaller problem sizes. This is also because of limitations in MLIR lowerings, this time from *scf.parallel* to the GPU dialect, where MLIR invokes a synchronous kernel execution for each parallel loop and thus execution across the CPU and GPU blocks at the end of each kernel.

Table 1 reports performance for both benchmarks on an Alveo U280 FPGA. We support FPGAs by the development of an MLIR *HLS* dialect and transformations [Rodriguez-Canal et al. 2023b] which lower from this to LLVM-IR and others which lower to the HLS dialect from the *stencil* dialect. LLVM-IR is then provided to the AMD Xilinx HLS

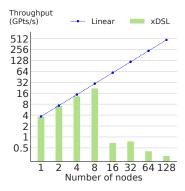
LLVM backend which synthesizes the corresponding kernel [Rodriguez-Canal et al. 2023a]. The *Initial* version represents the algorithm running on the FPGA unchanged from it's Von Neumann based CPU design, whereas the *optimized* version has been transformed by the compiler into a form tuned for dataflow architectures. This transformation has involved breaking the constituent components of the algorithm into separate dataflow regions and the use of a 3D shift buffer [Brown 2021] which is a bespoke cache that, when filled, enables all the current grid cell's stencil values to be provided to the calculation each cycle but one value needs to be read from DDR external memory per cycle. Ultimately, this means that calculation loops are able to be pipelined and run without stalling, computing a grid cell each cycle.

These performance numbers demonstrate two important benefits of our flow, firstly that we provide the ability to target FPGAs from a single Fortran source code, adding a new capability to PSyclone. Secondly, as can be seen by the performance improvement between optimized and initial versions in table 1, working with a high-level stencil description of the problem enables transformations to undertake automatic tuning to a dataflow architecture. Manual FPGA tuning is a very time-consuming step that requires considerable expertise [Brown 2020], and so the ability for xDSL to automatically undertake this provides an important capability that has the potential to enhance vendor tools. Whilst the FPGA numbers reported in table 1 fall short of the NVIDIA V100 GPU performance, these are not only in agreement with the performance of tuned PW advection manually optimized for FPGAs [Brown 2021], but it should also be highlighted that the MLIR GPU and CPU pipelines that we leverage are of production quality maturity and optimized by vendor teams.

Figure 11a reports the throughput for strong scaling of the PW advection benchmark on ARCHER2 up to 128 nodes (16384 cores). Unlike Devito, the PSyclone NEMO API we are using does not provide distributed memory capabilities, therefore, only xDSL-PSyclone results are presented here. The code was compiled with xDSL-PSyclone, and lowered using the *stencil*, *dmp* and *mpi* dialects, leveraging a 2D *dmp decomposition strategy*, which is commonplace in these types of model due to tight coupling in the vertical dimension. xDSL-PSyclone provides good strong scaling to eight nodes but then suffers from strong scaling effects due to the small global problem size. Likewise, fig. 11b reports throughput for the tracer advection benchmark where we observe similar behavior, with the 2D decomposition strategy limiting the strong scaling capability of xDSL-PSyclone.

7 Related Work

Numerous DSLs and compiler frameworks for HPC stencil computations exist. In contrast to building a siloed language and compiler infrastructure, our work differs from many previous attempts: we leverage the MLIR infrastructure to



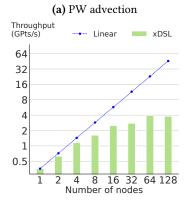


Figure 11. Multi-node strong scaling CPU throughput for xDSL-PSyclone for PW advection [256, 256, 128] (a) and tracer advection [512, 512, 128] (b) on ARCHER2 (higher is better)

(b) Tracer advection

share maintenance support and interoperability with other community-driven IRs. High-level approaches to problem modeling using symbolic notation include the Python-based OpenSBLI [Jacobs et al. 2017], using Einstein notation and the C/C++-based OPS library [Reguly et al. 2018] underneath for automated parallelism. ExaStencils [Kuckuk and Köstler 2016; Lengauer et al. 2020] has a multi-layered high-level symbolic DSL for FDs, targetting multi-CPU and multi-GPU. STELLA [Gysi et al. 2015] (and susbequently GridTools [Afanasyev et al. 2021]) uses a concise discretized mathematical syntax and helped port the COSMO model [Thaler et al. 2019] to NVIDIA GPUs.

Using a notation closer to modeling loops and arithmetic expressions, notable code-generation frameworks include Patus [Christen et al. 2011], the Pochoir stencil compiler [Tang et al. 2011], Physis [Maruyama et al. 2011] with C-based embedded DSL and Mint [Unat et al. 2011], a source-to-source translator for CUDA. MSC [Li et al. 2021] facilitates halo exchanges for DMP targeting many-core processor systems such as Sunway and Matrix. SDSLc [Rawat et al. 2015] targets CPUs and GPUs, Shift Calculus [Liao et al. 2015] differs by

using an ontology language. Lift [Steuwer et al. 2015], based upon semantic-preserving rewrite rules to optimize stencils, StencilGen [Rawat et al. 2018] targets GPUs with more exotic optimizations, such as overlapped temporal blocking, and Artemis [Rawat et al. 2019] primarily targets GPUs. Other efforts to benefit from MLIR include domain-specific code generators using tensor-level abstractions [Essadki et al. 2023].

Targetting diverse problem domains in science other than FD stencils, for unstructured meshes, we encounter OP2 [Mudalige et al. 2019; Reguly et al. 2016], Liszt [DeVito et al. 2011], Paralab/Finch [Heisler et al. 2023], Firedrake [Ham et al. 2023], UFL [Alnæs 2012] and FEniCS [Logg et al. 2012]. SPIRAL [Puschel et al. 2005] targets Digital Signal Processing and Tensor Contraction Engine [Auer et al. 2006] for molecular physics. On the medical applications side, MOD2IR [Mitenkov et al. 2023] focuses on neuronal simulations, leveraging the LLVM toolchain to facilitate the optimization of NMODL [Hines and Carnevale 2000]. limpetMLIR [Thangamani et al. 2023] uses MLIR and targets electrophysiology models, and Stride [Cueto et al. 2022], built on top of Devito, focuses on ultra-sound tomography imaging. For tensor algebra, TACO [Kjolstad et al. 2017] offers a high-level DSL targeting a range of hardware accelerators. On the image processing side, Halide [Denniston et al. 2016; Ragan-Kelley et al. 2013] is a toolkit for generating HPC codes from functional specifications in image processing using programmerspecified scheduling transformations, the polyhedral-based PolyMage [Mullapudi et al. 2015] offers a high-level Python DSL and optimizing code generator and Forma [Ravishankar et al. 2015] also targetting GPUs and claims to provide an easier-to-handle DSL interface.

Focusing more on libraries and frameworks optimizing loop-dominated codes, Python-based Loo.py [Klöckner 2014], generates code for OpenCL/CUDA, Chill [Chen et al. 2008] guides high-level loop transformations, YASK [Yount et al. 2016] specializing in data layout transformations to optimize for high-bandwidth Intel architectures. Numba [Lam et al. 2015] uses decorators for runtime-acceleration of Python code using LLVM as a backend. Notable annotation-based approaches include Tai-Chi [Hu et al. 2019] and DaCe [Ziogas et al. 2021].

Regarding frameworks to assist DSL developers in building DSLs for HPC code, AnyDSL [Leißa et al. 2018] provides composable DSL development using partial evaluation. Julia [Bezanson et al. 2017] combines dynamic types with the ability to generate HPC code. Python-based projects like Codon [Shajii et al. 2023], features static typing and compilation via LLVM, showcasing notable speedups compared to native Python routines and Mojo [Modular [n. d.]] as a Pythonic frontend for MLIR, displays a significant performance boost over state-of-the-art tools. Finally, the MSF's [Coullon et al. 2019] approach differs in addressing the sharing of common abstractions between stencil frameworks, providing a

stencil-DSL operating in an ahead-of-time non-embedded fashion.

Describing and optimizing communication patterns for DMP/MPI scientific software is a focus of many libraries and compilers [Castillo et al. 2019; Wang and Chandramowlishwaran 2020; Zhao et al. 2021, 2018]. Halide [Denniston et al. 2016], Exaslang [Kuckuk and Köstler 2016] and PETSc [Zhang et al. 2022] facilitate large-scale computational science with libraries supporting efficient execution at all parallelism levels (SIMD, SMP, DMP). Finally, *ParallelStencil.jl* [Omlin et al. 2022] is a high-level Julia approach using bindings for MPI *MPI.jl* [Byrne et al. 2021].

8 Conclusions and Future Work

By merging the backend compilation stacks of two stencil-DSLs focusing on FD stencils, PSyclone and Devito, we presented a prototype to support these important domainspecific abstractions and their optimizations that can be shared across DSLs. As a result, their developer communities can benefit from delivering peak performance for key applications reasoning about FD stencils, such as seismic and medical imaging and weather modeling, targeting CPUs, GPUs, and clusters thereof. To enable broad sharing of abstractions, we expressed fundamental HPC abstractions such as message passing and halo exchanges as SSA-based IRs for the MLIR compiler ecosystem. We demonstrated that these abstractions enable the generation of code employing shared and distributed parallelism exhibiting competitive single-node and strong scaling performance to state-of-theart supercomputers. The MPI abstractions are generic and independent of the specific application domain, while the DMP abstractions are focused on halo exchanges specific to FD stencil computations. Both enable the sharing of optimizations and code generation strategies for message passing across stencil computations that target supercomputers. Our evaluation across stencil kernel workloads from Devito and PSyclone shows competitive and even improved performance while broadening the set of targets.

We hope that this work on HPC abstractions for MPI and distributed-memory code generation transcends the specific application domains of our DSLs and motivates further research on exploiting synergies enabled by collaborations across DSL and compiler frameworks in HPC. We aim to establish a cohesive ecosystem of HPC-oriented IRs within the compiler landscape, facilitating reasoning and HPC code generation. These IRs promote modularity and interoperability by abstracting away from domain-specific considerations, aiming to enable code generation for efficient and scalable codes across DSLs targeting problems other than stencils.

A limitation identified by our benchmarking has been in the existing MLIR lowerings from the *scf* dialect to the OpenMP and GPU dialects. Further work optimizing these would be beneficial, potentially requiring developing bespoke lowerings which are able to consider the wider context that an *scf.parallel* operation sits within. The ability to support one parallel region across all *scf.parallel* loops in OpenMP and finer-grained control over the synchronization of GPU kernels are important aspects that would likely deliver significant performance improvements for codes like the tracer advection benchmark. Further work includes enhancing the decomposition techniques to support advanced exchange schemes and DMP/MPI optimizations, such as diagonal communications in the cartesian grid topology and communication/computation overlap. The abstractions presented in this paper aim to be modular and extensible building blocks to facilitate these future developments.

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