The *Lift* Project: Performance Portable GPU Code Generation via Rewrite Rules

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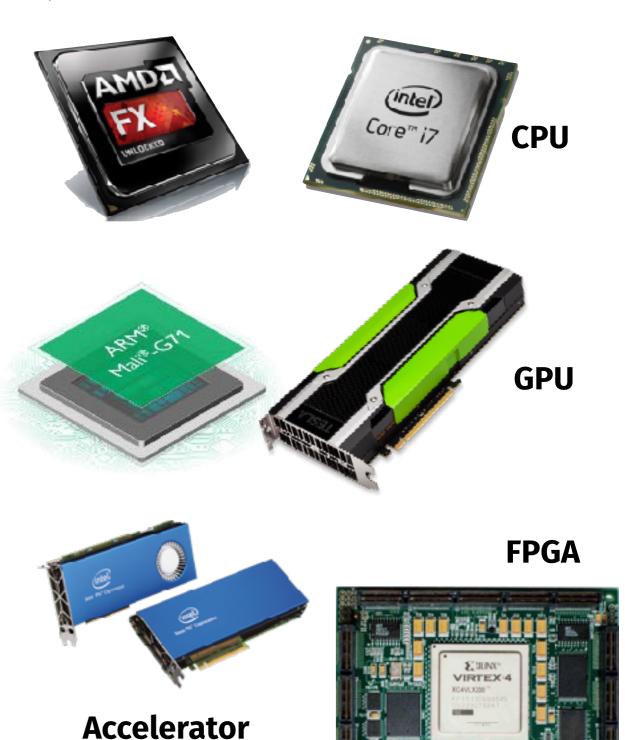
http://www.lift-project.org/





What are the problems Lift tries to tackle?

- Parallel processors everywhere
- Many different types: CPUs, GPUs, ...
- Parallel programming is hard
- Optimising is even harder
- Problem:No portability of performance!



Prologue

To achieve performance portability we *need* high-level abstraction!

Traditional imperative programming approaches *always* lead to non-portable code

Traditional compiler & runtimes have no freedom to explore alternative implementations

Lessons from the past

1968

A Case against the GO TO Statement.

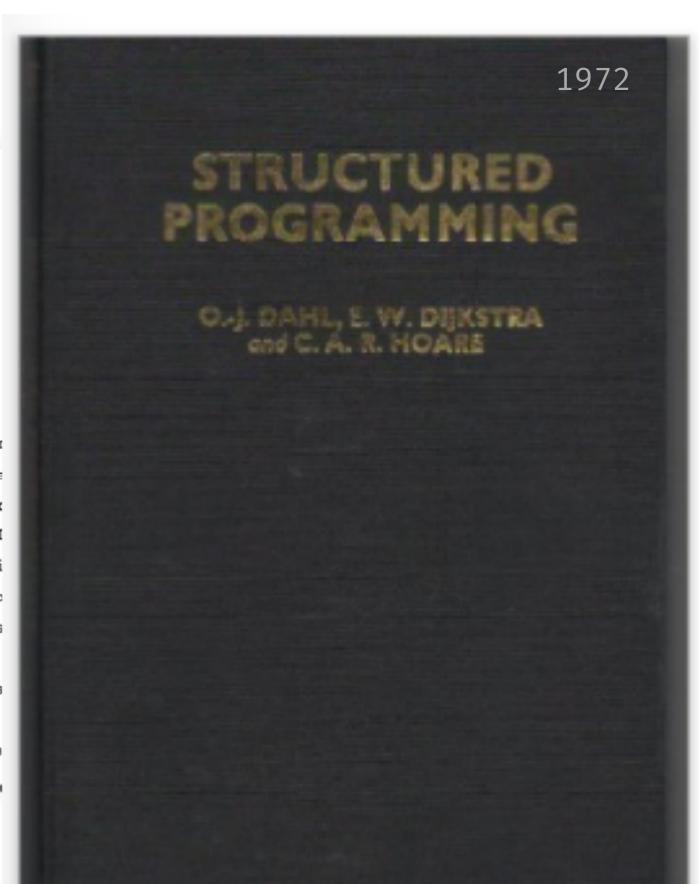
by Edsger W.Dijkotra

Technological University

Eindhoven, The Netherlands

Since a number of years I am familiar with the obser quality of programmers is a decreasing function of the destatements in the programs they produce. Later I discover the go to statement has such disastrous effects and did I that the go to statement should be abolished from all "hi programming languages (i.e. everything except -perhaps- p At that time I did not attach too much importance to this submit my considerations for publication because in very in which the subject turned up, I have been urged to do s

My first remark is that, although the programmer's a he has constructed a correct program, the process taking



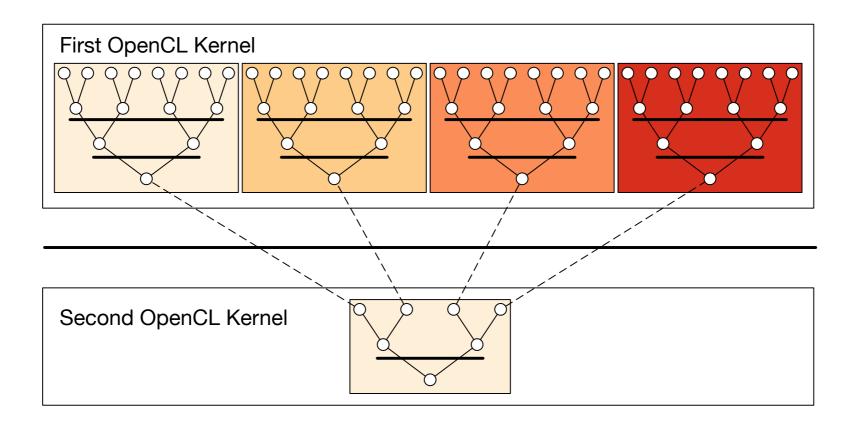
"High-level" abstractions like if and for have carried us through the sequential age of computing

We need appropriate high-level abstractions for the parallel and concurrent age of computing

End of Prologue

Case Study: Parallel Reduction in OpenCL

- Summing up all values of an array
- Comparison of 7 implementations by Nvidia
- Investigating complexity and efficiency of optimisations



• Case Study: Parallel reduction in OpenCL

• Case Study: Parallel reduction in OpenCL

Kernel function executed in parallel by multiple work-items

Work-items are identified by a unique global id

• Case Study: Parallel reduction in OpenCL

Work-items are grouped into work-groups

Local id within work-group

Case Study: Parallel reduction in OpenCL

Big, but slow **global** memory

Small, but fast **local** memory

Memory **barriers** for consistency

• Case Study: Parallel reduction in OpenCL

Functionally correct implementations in OpenCL are hard!

Unoptimised Implementation Parallel Reduction

```
kernel void reduce0(global float* g_idata, global float* g_odata,
                    unsigned int n, local float* l_data) {
  unsigned int tid = get_local_id(0);
  unsigned int i = get_global_id(0);
  l data[tid] = (i < n) ? g idata[i] : 0;</pre>
  barrier(CLK_LOCAL_MEM_FENCE);
 // do reduction in local memory
  for (unsigned int s=1; s < get_local_size(0); s*= 2) {</pre>
    if ((tid % (2*s)) == 0) {
      l_data[tid] += l_data[tid + s];
    barrier(CLK_LOCAL_MEM_FENCE);
  // write result for this work-group to global memory
  if (tid == 0) g_odata[get_group_id(0)] = l_data[0];
```

Avoid Divergent Branching

```
kernel void reduce1(global float* g_idata, global float* g_odata,
                     unsigned int n, local float* l_data) {
  unsigned int tid = get_local_id(0);
  unsigned int i = get_global_id(0);
  l data[tid] = (i < n) ? g idata[i] : 0;</pre>
  barrier(CLK_LOCAL_MEM_FENCE);
  for (unsigned int s=1; s < get_local_size(0); s*= 2) {</pre>
    // continuous work-items remain active
    int index = 2 * s * tid;
    if (index < get_local_size(0)) {</pre>
      l_data[index] += l_data[index + s];
    barrier(CLK_LOCAL_MEM_FENCE);
  if (tid == 0) g_odata[get_group_id(0)] = l_data[0];
```

Avoid Interleaved Addressing

```
kernel void reduce2(global float* g_idata, global float* g_odata,
                    unsigned int n, local float* l_data) {
  unsigned int tid = get_local_id(0);
  unsigned int i = get_global_id(0);
 l_data[tid] = (i < n) ? g_idata[i] : 0;</pre>
  barrier(CLK_LOCAL_MEM_FENCE);
 // process elements in different order
 // requires commutativity
  for (unsigned int s=get_local_size(0)/2; s>0; s>>=1) {
    if (tid < s) {
      l_data[tid] += l_data[tid + s];
    barrier(CLK_LOCAL_MEM_FENCE);
  if (tid == 0) g_odata[get_group_id(0)] = l_data[0];
```

Increase Computational Intensity per Work-Item

```
kernel void reduce3(global float* g_idata, global float* g_odata,
                    unsigned int n, local float* l_data) {
  unsigned int tid = get_local_id(0);
  unsigned int i = get_group_id(0) * (get_local_size(0)*2)
                                    + get_local_id(0);
  l data[tid] = (i < n) ? g idata[i] : 0;</pre>
  // performs first addition during loading
  if (i + get local size(0) < n)
    l_data[tid] += g_idata[i+get_local_size(0)];
  barrier(CLK_LOCAL_MEM_FENCE);
  for (unsigned int s=get_local_size(0)/2; s>0; s>>=1) {
    if (tid < s) {
      l_data[tid] += l_data[tid + s];
    barrier(CLK_LOCAL_MEM_FENCE);
  if (tid == 0) g_odata[get_group_id(0)] = l_data[0];
```

Avoid Synchronisation inside a Warp

```
kernel void reduce4(global float* g_idata, global float* g_odata,
                    unsigned int n, local volatile float* l_data) {
  unsigned int tid = get_local_id(0);
  unsigned int i = get_group_id(0) * (get_local_size(0)*2)
                                    + get_local_id(0);
 l_data[tid] = (i < n) ? g_idata[i] : 0;</pre>
 if (i + get_local_size(0) < n)</pre>
    l_data[tid] += g_idata[i+get_local_size(0)];
  barrier(CLK_LOCAL_MEM_FENCE);
  # pragma unroll 1
  for (unsigned int s=get_local_size(0)/2; s>32; s>>=1) {
    if (tid < s) { l data[tid] += l data[tid + s]; }</pre>
    barrier(CLK_LOCAL_MEM_FENCE); }
 // this is not portable OpenCL code!
 if (tid < 32) {
    if (WG SIZE >= 64) { l data[tid] += l data[tid+32]; }
    if (WG_SIZE >= 32) { l_data[tid] += l_data[tid+16]; }
    if (WG_SIZE >= 16) { l_data[tid] += l_data[tid+ 8]; }
    if (WG_SIZE >= 8) { l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) { l data[tid] += l data[tid+ 2]; }
    if (WG_SIZE >= 2) { l_data[tid] += l_data[tid+ 1]; } }
  if (tid == 0) g odata[get_group_id(0)] = l data[0]; }
```

Complete Loop Unrolling

```
kernel void reduce5(global float* g_idata, global float* g_odata,
                    unsigned int n, local volatile float* l data) {
  unsigned int tid = get_local_id(0);
  unsigned int i = get_group_id(0) * (get_local_size(0)*2)
                                    + get_local_id(0);
  l_data[tid] = (i < n) ? g_idata[i] : 0;</pre>
  if (i + get_local_size(0) < n)</pre>
    l_data[tid] += g_idata[i+get_local_size(0)];
  barrier(CLK_LOCAL_MEM_FENCE);
  if (WG SIZE >= 256) {
    if (tid < 128) { l data[tid] += l data[tid+128]; }</pre>
    barrier(CLK_LOCAL_MEM_FENCE); }
  if (WG SIZE >= 128) {
    if (tid < 64) { l_data[tid] += l_data[tid+ 64]; }</pre>
    barrier(CLK_LOCAL_MEM_FENCE); }
  if (tid < 32) {
    if (WG_SIZE >= 64) { l_data[tid] += l_data[tid+32]; }
    if (WG_SIZE >= 32) { l_data[tid] += l_data[tid+16]; }
    if (WG_SIZE >= 16) { l_data[tid] += l_data[tid+ 8]; }
    if (WG_SIZE >= 8) { l_data[tid] += l_data[tid+ 4]; }
    if (WG_SIZE >= 4) { l_data[tid] += l_data[tid+ 2]; }
    if (WG_SIZE >= 2) { l_data[tid] += l_data[tid+ 1]; } }
  if (tid == 0) g_odata[get_group_id(0)] = l_data[0]; }
```

Fully Optimised Implementation

```
kernel void reduce6(global float* g_idata, global float* g_odata,
                    unsigned int n, local volatile float* l_data) {
  unsigned int tid = get local id(0);
  unsigned int i = get_group_id(0) * (get_local_size(0)*2)
                                    + get_local_id(0);
  unsigned int gridSize = WG_SIZE * get_num_groups(0);
  l data[tid] = 0;
  while (i < n) { l_data[tid] += g_idata[i];</pre>
                  if (i + WG_SIZE < n)</pre>
                    l_data[tid] += g_idata[i+WG_SIZE];
                  i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
  if (WG SIZE >= 256) {
    if (tid < 128) { l_data[tid] += l_data[tid+128]; }</pre>
    barrier(CLK_LOCAL_MEM_FENCE); }
  if (WG_SIZE >= 128) {
    if (tid < 64) { l_data[tid] += l_data[tid+ 64]; }</pre>
    barrier(CLK_LOCAL_MEM_FENCE); }
  if (tid < 32) {
    if (WG_SIZE >= 64) { l_data[tid] += l_data[tid+32]; }
    if (WG_SIZE >= 32) { l_data[tid] += l_data[tid+16]; }
    if (WG_SIZE >= 16) { l_data[tid] += l_data[tid+ 8]; }
    if (WG_SIZE >= 8) { l_data[tid] += l_data[tid+ 4]; }
    if (WG_SIZE >= 4) { l_data[tid] += l_data[tid+ 2]; }
    if (WG_SIZE >= 2) { l_data[tid] += l_data[tid+ 1]; } }
  if (tid == 0) g_odata[get_group_id(0)] = l_data[0]; }
```

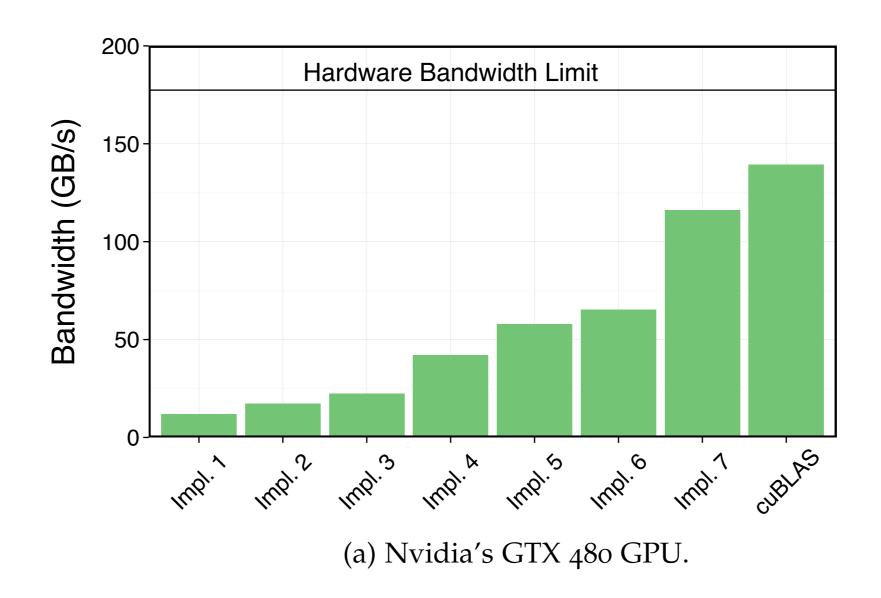
Case Study Conclusions

- Optimising OpenCL is complex
 - Understanding of target hardware required
- Program changes not obvious
- Is it worth it? ...

```
kernel
void reduce0(global float* g_idata,
             global float* g odata,
             unsigned int n,
             local float* l data) {
 unsigned int tid = get local id(0);
 unsigned int i = get_global_id(0);
 l_data[tid] = (i < n) ? g_idata[i] : 0;</pre>
 barrier(CLK LOCAL MEM FENCE);
 for (unsigned int s=1;
       s < get local size(0); s*= 2) {
   if ((tid \% (2*s)) == 0) {
      l data[tid] += l data[tid + s];
    barrier(CLK_LOCAL_MEM_FENCE);
 if (tid == 0)
   g_odata[get_group_id(0)] = l_data[0];
```

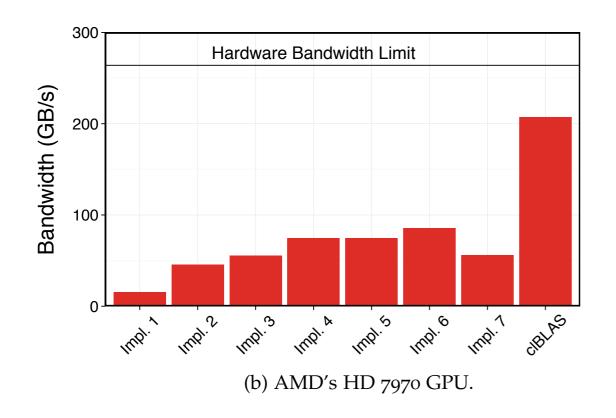
```
kernel
void reduce6(global float* g_idata,
             global float* g_odata,
             unsigned int n,
             local volatile float* l data) {
  unsigned int tid = get_local_id(0);
  unsigned int i =
   get group id(0) * (get local size(0)*2)
                    + get_local_id(0);
  unsigned int gridSize =
    WG SIZE * get num groups(0);
  l_data[tid] = 0;
  while (i < n) {
   l data[tid] += g idata[i];
   if (i + WG SIZE < n)</pre>
     l data[tid] += g idata[i+WG SIZE];
    i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
 if (WG_SIZE >= 256) {
   if (tid < 128) {
      l data[tid] += l data[tid+128]; }
   barrier(CLK LOCAL MEM FENCE); }
  if (WG_SIZE >= 128) {
    if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
  if (tid < 32) {
    if (WG SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
    if (WG SIZE >= 32) {
     l data[tid] += l data[tid+16]; }
    if (WG SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
     l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) {
     l_data[tid] += l_data[tid+ 2]; }
    if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
  if (tid == 0)
   g_odata[get_group_id(0)] = l_data[0];
```

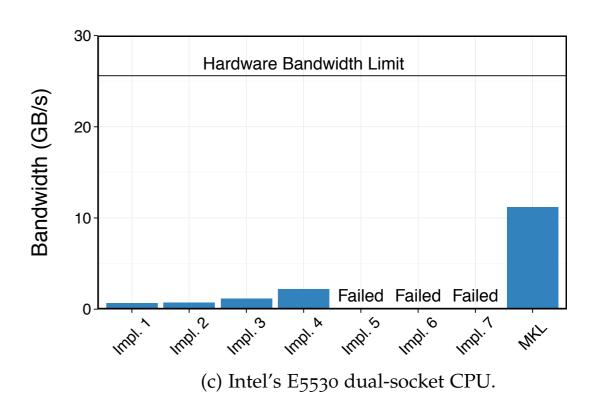
Performance Results Nvidia



- ... Yes! Optimising improves performance by a factor of 10!
- Optimising is important, but ...

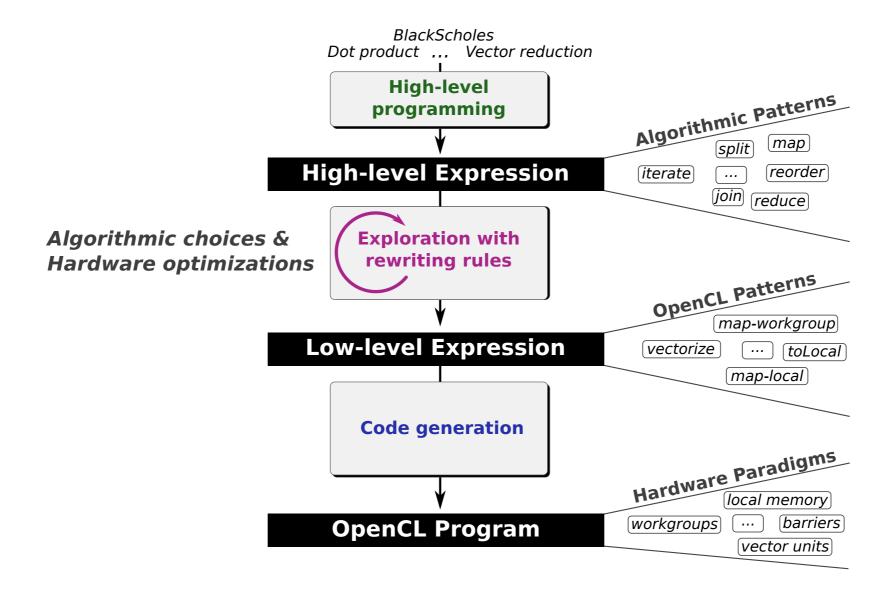
Performance Results AMD and Intel





- ... unfortunately, optimisations in OpenCL are not portable!
- Challenge: how to achieving portable performance?

Lift: Performance Portable GPU Code Generation via Rewrite Rules



Ambition: automatic generation of Performance Portable code

Michel Steuwer, Christian Fensch, Sam Lindley, and Christophe Dubach "Generating Performance Portable Code using Rewrite Rules: From High-Level Functional Expressions to High-Performance OpenCL Code" in ICFP 2015.

Walkthrough

rewrite rules

code generation

```
2
```

```
vecSum = reduce o join o map-workgroup (
    join o toGlobal (map-local (map-seq id)) o split 1 o
    join o map-warp (
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 1 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 2 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 4 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 8 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 16 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 32
      ) o split 64 o
        join o map-local (reduce-seq (+) 0) o split 2 o reorder-stride 64 o
        join o toLocal (map-local (reduce-seq (+) 0)) o
        split (blockSize/128) o reorder-stride 128
     ) o split blockSize
```

```
kernel
void reduce6(global float* g_idata,
             global float* g_odata,
             unsigned int n,
             local volatile float* l data) {
  unsigned int tid = get_local_id(0);
  unsigned int i =
   get_group_id(0) * (get_local_size(0)*2)
                    + get_local_id(0);
  unsigned int gridSize =
   WG_SIZE * get_num_groups(0);
 l_data[tid] = 0;
  while (i < n) {
   l data[tid] += g idata[i];
    if (i + WG SIZE < n)</pre>
     l_data[tid] += g_idata[i+WG_SIZE];
    i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
 if (WG_SIZE >= 256) {
   if (tid < 128) {
     l_data[tid] += l_data[tid+128]; }
    barrier(CLK LOCAL MEM FENCE); }
  if (WG_SIZE >= 128) {
    if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
  if (tid < 32) {
    if (WG SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
    if (WG SIZE >= 32) {
     l_data[tid] += l_data[tid+16]; }
    if (WG SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
      l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) {
     l_data[tid] += l_data[tid+ 2]; }
    if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
  if (tid == 0)
   g_odata[get_group_id(0)] = l_data[0];
```

Walkthrough

sum(vec) = reduce(+, 0, vec)

rewrite rules code generation



```
vecSum = reduce o join o map-workgroup
      join o toGlobal (map-local (map-seg id)) o split 1 o
      join o map-warp (
        join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 1 ∘
        join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 2 ∘
        join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 4 ∘
        join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 8 ∘
        join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 16 ∘
        join ∘ map-lane (reduce-seg (+) 0) ∘ split 2 ∘ reorder-stride 32
      ) o split 64 o
      join o map-local (reduce-seq (+) 0) o split 2 o reorder-stride 64 o
      join ∘ toLocal (map-local (reduce-seg (+) 0)) ∘
     split (blockSize/128) o reorder-stride 128
   osplit blockSize
```

```
kernel
void reduce6(global float* g idata,
             global float* g_odata,
             unsigned int n,
             local volatile float* l data) {
  unsigned int tid = get local id(0);
  unsigned int i =
    get group id(0) * (get local size(0)*2)
                    + get_local_id(0);
  unsigned int gridSize =
   WG SIZE * get num groups(0);
  l_data[tid] = 0;
 while (i < n) {
   l data[tid] += g idata[i];
   if (i + WG SIZE < n)</pre>
     l data[tid] += g idata[i+WG SIZE];
   i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
  if (WG_SIZE >= 256) {
   if (tid < 128) {
      l data[tid] += l data[tid+128]; }
    barrier(CLK LOCAL MEM FENCE); }
  if (WG_SIZE >= 128) {
   if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
  if (tid < 32) {
   if (WG SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
   if (WG SIZE >= 32) {
      l data[tid] += l data[tid+16]; }
    if (WG SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
      l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) {
     l_data[tid] += l_data[tid+ 2]; }
    if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
  if (tid == 0)
   g_odata[get_group_id(0)] = l_data[0];
```

1 Algorithmic Primitives (a.k.a. algorithmic skeletons)

map(f, x):	$\begin{bmatrix} x_1 & x_2 & x_3 & x_4 & x_5 & x_6 & x_7 & x_8 \end{bmatrix}$	$ f(x_1) f(x_2) f(x_3) f(x_4) f(x_5) f(x_6) f(x_7) f(x_8) $
zip(x, y):	$\begin{bmatrix} x_1 & x_2 & x_3 & x_4 & x_5 & x_6 & x_7 & x_8 \\ y_1 & y_2 & y_3 & y_4 & y_5 & y_6 & y_7 & y_8 \end{bmatrix}$	$ \longrightarrow (x_1, y_1)(x_2, y_2)(x_3, y_3)(x_4, y_4)(x_5, y_5)(x_6, y_6)(x_7, y_7)(x_8, y_6) $
reduce(+, 0, x):	$\begin{bmatrix} x_1 & x_2 & x_3 & x_4 & x_5 & x_6 & x_7 & x_8 \end{bmatrix}$	$\longrightarrow $
split(n, x):	$\begin{bmatrix} x_1 & x_2 & x_3 & x_4 & x_5 & x_6 & x_7 & x_8 \end{bmatrix}$	$\longrightarrow \begin{array}{ c c c c c c c c c c c c c c c c c c c$
join(x):	$\begin{bmatrix} x_1 & x_2 & x_3 & x_4 & x_5 & x_6 \end{bmatrix} \begin{bmatrix} x_7 & x_8 \end{bmatrix}$	$\longmapsto \begin{array}{c c c c c c c c c c c c c c c c c c c $
iterate(f, n, x):	$\begin{bmatrix} x_1 & x_2 & x_3 & x_4 & x_5 & x_6 & x_7 & x_8 \end{bmatrix}$	$\longmapsto f(\dots f(\boxed{x_1 x_2 x_3 x_4 x_5 x_6 x_7 x_8})\dots$
reorder(σ , x):	$\begin{bmatrix} x_1 & x_2 & x_3 & x_4 & x_5 & x_6 & x_7 & x_8 \end{bmatrix}$	$\longrightarrow \qquad \qquad x_{\sigma(1)} x_{\sigma(2)} x_{\sigma(3)} x_{\sigma(4)} x_{\sigma(5)} x_{\sigma(6)} x_{\sigma(7)} x_{\sigma(8)}$

1 High-Level Programs

```
scal(a, vec) = map(\lambda x \mapsto x*a, vec)
asum(vec) = reduce(+, 0, map(abs, vec))
dotProduct(x, y) = reduce(+, 0, map(*, zip(x, y)))
gemv(mat, x, y, \alpha, \beta) =
  map(+, zip(
     map(\lambda row \rightarrow scal(\alpha, dotProduct(row, x)), mat),
     scal(\beta, y))
```

Walkthrough

rewrite rules

code generation

```
2
```

```
vecSum = reduce o join o map-workgroup (
    join o toGlobal (map-local (map-seq id)) o split 1 o
    join o map-warp (
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 1 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 2 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 4 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 8 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 16 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 32
      ) o split 64 o
        join o map-local (reduce-seq (+) 0) o split 2 o reorder-stride 64 o
        join o toLocal (map-local (reduce-seq (+) 0)) o
        split (blockSize/128) o reorder-stride 128
     ) o split blockSize
```

```
kernel
void reduce6(global float* g_idata,
             global float* g_odata,
             unsigned int n,
             local volatile float* l data) {
  unsigned int tid = get_local_id(0);
  unsigned int i =
   get_group_id(0) * (get_local_size(0)*2)
                    + get_local_id(0);
  unsigned int gridSize =
   WG_SIZE * get_num_groups(0);
 l_data[tid] = 0;
  while (i < n) {
   l data[tid] += g idata[i];
    if (i + WG SIZE < n)</pre>
     l_data[tid] += g_idata[i+WG_SIZE];
    i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
 if (WG_SIZE >= 256) {
   if (tid < 128) {
     l_data[tid] += l_data[tid+128]; }
    barrier(CLK LOCAL MEM FENCE); }
  if (WG_SIZE >= 128) {
    if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
  if (tid < 32) {
    if (WG SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
    if (WG SIZE >= 32) {
     l_data[tid] += l_data[tid+16]; }
    if (WG SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
      l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) {
     l_data[tid] += l_data[tid+ 2]; }
    if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
  if (tid == 0)
   g_odata[get_group_id(0)] = l_data[0];
```

Walkthrough

3

1) sum(vec) = reduce(+, 0, vec)

rewrite rules

rewrite rules code generation

2

```
vecSum = reduce o join o map-workgroup (
    join o toGlobal (map-local (map-seq id)) o split 1 o
    join o map-warp (
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 1 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 2 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 4 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 8 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 16 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 32
        ) o split 64 o
        join o map-local (reduce-seq (+) 0) o split 2 o reorder-stride 64 o
        join o toLocal (map-local (reduce-seq (+) 0)) o
        split (blockSize/128) o reorder-stride 128
        ) o split blockSize
```

```
kernel
void reduce6(global float* g idata,
             global float* g_odata,
             unsigned int n,
             local volatile float* l data) {
  unsigned int tid = get local id(0);
  unsigned int i =
    get group id(0) * (get local size(0)*2)
                    + get_local_id(0);
  unsigned int gridSize =
   WG SIZE * get num groups(0);
  l_data[tid] = 0;
 while (i < n) {
   l data[tid] += g idata[i];
   if (i + WG SIZE < n)</pre>
     l data[tid] += g idata[i+WG SIZE];
   i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
 if (WG_SIZE >= 256) {
   if (tid < 128) {
     l_data[tid] += l_data[tid+128]; }
    barrier(CLK LOCAL MEM FENCE); }
  if (WG_SIZE >= 128) {
   if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
    barrier(CLK_LOCAL_MEM_FENCE); }
  if (tid < 32) {
   if (WG SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
   if (WG SIZE >= 32) {
      l data[tid] += l data[tid+16]; }
   if (WG SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
      l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) {
     l_data[tid] += l_data[tid+ 2]; }
    if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
  if (tid == 0)
   g_odata[get_group_id(0)] = l_data[0];
```

2 Algorithmic Rewrite Rules

- Provably correct rewrite rules
- Express algorithmic implementation choices

Split-join rule:

```
map \ f \rightarrow join \circ map \ (map \ f) \circ split \ n
```

Map fusion rule:

```
map \ f \circ map \ g \to map \ (f \circ g)
```

Reduce rules:

```
reduce f \ z \to reduce \ f \ z \circ reduce Part \ f \ z

reduce Part \ f \ z \to reduce Part \ f \ z \circ reorder

reduce Part \ f \ z \to join \ \circ map \ (reduce Part \ f \ z) \circ split \ n

reduce Part \ f \ z \to iterate \ n \ (reduce Part \ f \ z)
```

2 OpenCL Primitives

Primitive

OpenCL concept

mapGlobal

Work-items

workgroups global threads

 $map\,Work group$

mapLocal

Work-groups

mapSeq

reduceSeq

Sequential implementations

toLocal , toGlobal

Memory areas

map Vec, split Vec, join Vec

Vectorisation

2 OpenCL Rewrite Rules

Express low-level implementation and optimisation choices

Map rules:

```
map\ f \rightarrow map\ Workgroup\ f \mid map\ Local\ f \mid map\ Global\ f \mid map\ Seq\ f
```

Local/ global memory rules:

```
mapLocal\ f \rightarrow toLocal\ (mapLocal\ f) mapLocal\ f \rightarrow toGlobal\ (mapLocal\ f)
```

Vectorisation rule:

```
map\ f \rightarrow join\ Vec \circ map\ (map\ Vec\ f) \circ split\ Vec\ n
```

Fusion rule:

$$reduceSeq\ f\ z\circ mapSeq\ g\to reduceSeq\ (\lambda\ (acc,x).\ f\ (acc,g\ x))\ z$$

Walkthrough

) vecSum = reduce (+) 0

rewrite rules



(2)

```
vecSum = reduce o join o map-workgroup (
    join o toGlobal (map-local (map-seq id)) o split 1 o
    join o map-warp (
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 1 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 2 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 4 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 8 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 16 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 32
      ) o split 64 o
        join o map-local (reduce-seq (+) 0) o split 2 o reorder-stride 64 o
        join o toLocal (map-local (reduce-seq (+) 0)) o
        split (blockSize/128) o reorder-stride 128
     ) o split blockSize
```

```
kernel
void reduce6(global float* g_idata,
             global float* g_odata,
             unsigned int n,
             local volatile float* l data) {
  unsigned int tid = get_local_id(0);
  unsigned int i =
   get_group_id(0) * (get_local_size(0)*2)
                    + get_local_id(0);
  unsigned int gridSize =
   WG_SIZE * get_num_groups(0);
 l_data[tid] = 0;
  while (i < n) {
   l data[tid] += g idata[i];
    if (i + WG SIZE < n)</pre>
     l_data[tid] += g_idata[i+WG_SIZE];
    i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
 if (WG_SIZE >= 256) {
   if (tid < 128) {
     l_data[tid] += l_data[tid+128]; }
    barrier(CLK LOCAL MEM FENCE); }
  if (WG_SIZE >= 128) {
    if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
  if (tid < 32) {
    if (WG SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
    if (WG SIZE >= 32) {
     l_data[tid] += l_data[tid+16]; }
    if (WG SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
      l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) {
     l_data[tid] += l_data[tid+ 2]; }
    if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
  if (tid == 0)
   g_odata[get_group_id(0)] = l_data[0];
```

Walkthrough



rewrite rules code generation



```
vecSum = reduce o join o map-workgroup
      join o toGlobal (map-local (map-seg id)) o split 1 o
      join o map-warp (
        join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 1 ∘
        join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 2 ∘
        join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 4 ∘
        join ∘ map-lane (reduce-seg (+) 0) ∘ split 2 ∘ reorder-stride 8 ∘
        join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 16 ∘
        join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 32
      ) o split 64 o
      join o map-local (reduce-seq (+) 0) o split 2 o reorder-stride 64 o
      join ∘ toLocal (map-local (reduce-seg (+) 0)) ∘
     split (blockSize/128) o reorder-stride 128
   osplit blockSize
```

```
kernel
void reduce6(global float* g_idata,
             global float* g_odata,
             unsigned int n,
             local volatile float* l data) {
  unsigned int tid = get_local_id(0);
  unsigned int i =
   get_group_id(0) * (get_local_size(0)*2)
                    + get_local_id(0);
  unsigned int gridSize =
   WG_SIZE * get_num_groups(0);
 l_data[tid] = 0;
  while (i < n) {
   l data[tid] += g idata[i];
    if (i + WG SIZE < n)</pre>
     l_data[tid] += g_idata[i+WG_SIZE];
    i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
 if (WG_SIZE >= 256) {
    if (tid < 128) {
     l_data[tid] += l_data[tid+128]; }
   barrier(CLK LOCAL MEM FENCE); }
  if (WG_SIZE >= 128) {
    if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
  if (tid < 32) {
    if (WG SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
    if (WG SIZE >= 32) {
      l data[tid] += l data[tid+16]; }
    if (WG SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
     l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) {
     l_data[tid] += l_data[tid+ 2]; }
    if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
  if (tid == 0)
    g_odata[get_group_id(0)] = l_data[0];
```

3 Pattern based OpenCL Code Generation

Generate OpenCL code for each OpenCL primitive

```
mapGlobal\ f\ xs \longrightarrow \begin{cases} \textbf{for (int g_id = get_global_id(0); g_id < n; g_id += get_global_size(0)) } \\ \text{output[g_id] = } \textbf{f(xs[g_id]);} \end{cases}
```

```
reduceSeq f z xs \longrightarrow \begin{cases} \text{T acc = z;} \\ \text{for (int i = 0; i < n; ++i) } \\ \text{acc = f(acc, xs[i]);} \end{cases}
```

•

 A lot more details about the code generation implementation can be found in our <u>CGO 2017 paper</u>

Walkthrough

) vecSum = reduce (+) 0

rewrite rules

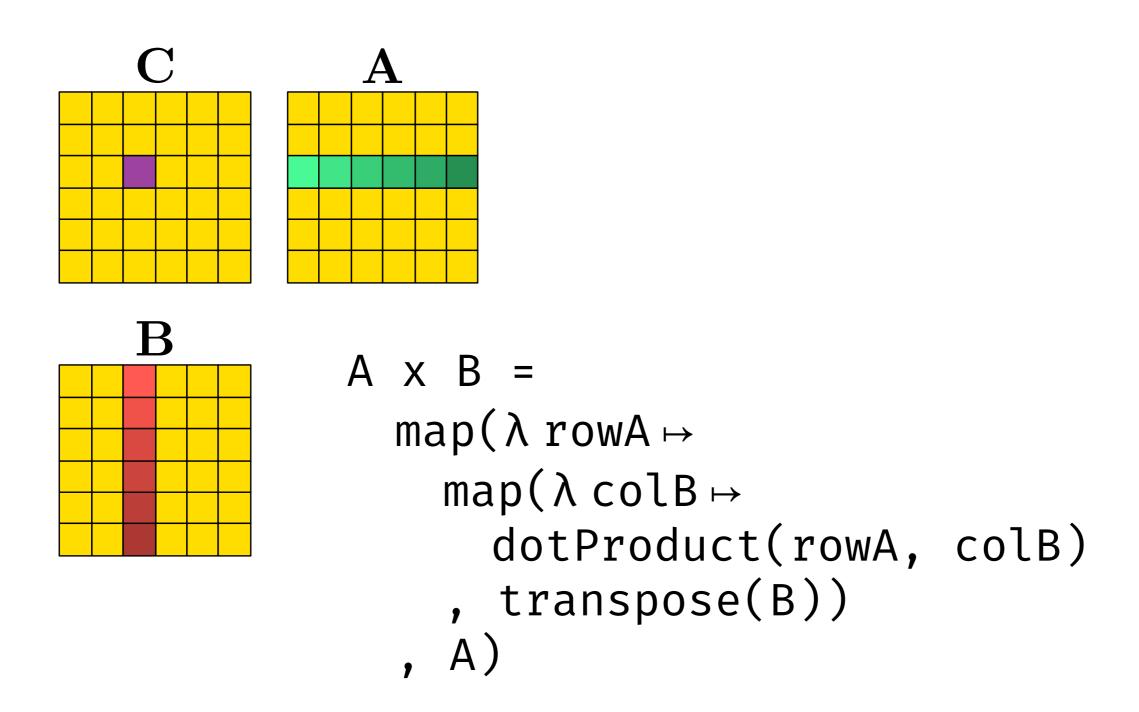


2

```
vecSum = reduce o join o map-workgroup (
    join o toGlobal (map-local (map-seq id)) o split 1 o
    join o map-warp (
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 1 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 2 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 4 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 8 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 16 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 32
      ) o split 64 o
        join o map-local (reduce-seq (+) 0) o split 2 o reorder-stride 64 o
        join o toLocal (map-local (reduce-seq (+) 0)) o
        split (blockSize/128) o reorder-stride 128
     ) o split blockSize
```

```
kernel
void reduce6(global float* g_idata,
             global float* g_odata,
             unsigned int n,
             local volatile float* l data) {
  unsigned int tid = get_local_id(0);
  unsigned int i =
   get_group_id(0) * (get_local_size(0)*2)
                    + get_local_id(0);
  unsigned int gridSize =
   WG_SIZE * get_num_groups(0);
 l_data[tid] = 0;
  while (i < n) {
   l data[tid] += g idata[i];
    if (i + WG SIZE < n)</pre>
     l_data[tid] += g_idata[i+WG_SIZE];
    i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
 if (WG_SIZE >= 256) {
   if (tid < 128) {
     l_data[tid] += l_data[tid+128]; }
    barrier(CLK LOCAL MEM FENCE); }
  if (WG_SIZE >= 128) {
    if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
  if (tid < 32) {
    if (WG SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
    if (WG SIZE >= 32) {
     l_data[tid] += l_data[tid+16]; }
   if (WG_SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
      l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) {
     l_data[tid] += l_data[tid+ 2]; }
    if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
  if (tid == 0)
   g_odata[get_group_id(0)] = l_data[0];
```

Case Study: Matrix Multiplication



Tiling as a Rewrite Rules

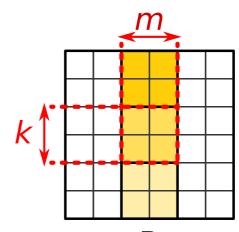
Naïve matrix multiplication

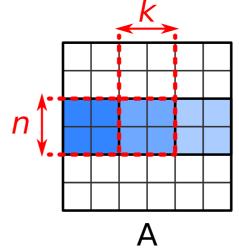
```
1 \quad map(\lambda \ arow \ .
2 \quad map(\lambda \ bcol \ .
3 \quad reduce(+, 0) \circ map(\times) \circ zip(arow, bcol)
4 \quad , transpose(B))
5 \quad , A)
```

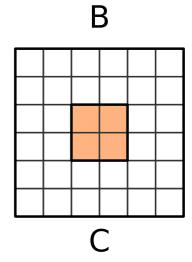


Apply tiling rules

```
untile \circ map(\lambda rowOfTilesA.
 1
       map(\lambda \ colOfTilesB.
 3
        toGlobal(copy2D) o
        reduce(\lambda (tileAcc, (tileA, tileB)).
 4
 5
         map(map(+)) \circ zip(tileAcc) \circ
         map(\lambda as.
 6
          map(\lambda bs).
            reduce(+, 0) \circ map(\times) \circ zip(as, bs)
 8
           , toLocal(copy2D(tileB)))
 9
         , toLocal(copy2D(tileA)))
10
        ,0, zip(rowOfTilesA, colOfTilesB))
11
       ) \circ tile(m, k, transpose(B))
12
      ) \circ tile(n, k, A)
13
```





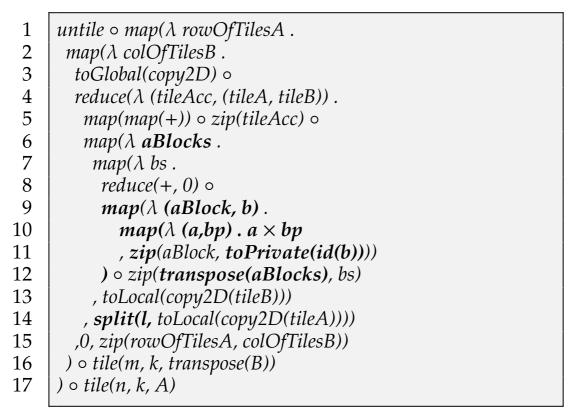


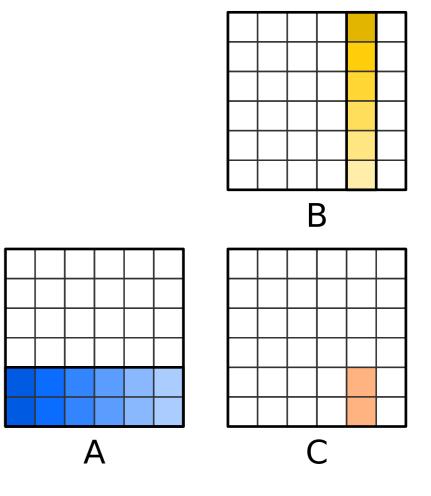
Register Blocking as a Rewrite Rules

```
untile \circ map(\lambda rowOfTilesA.
       map(\lambda \ colOfTilesB.
        toGlobal(copy2D) o
 3
 4
        reduce(\lambda (tileAcc, (tileA, tileB)).
 5
         map(map(+)) \circ zip(tileAcc) \circ
         map(\lambda as.
 6
 7
          map(\lambda bs).
 8
            reduce(+, 0) \circ map(\times) \circ zip(as, bs)
          , toLocal(copy2D(tileB)))
 9
10
         , toLocal(copy2D(tileA)))
        ,0, zip(rowOfTilesA, colOfTilesB))
11
12
       ) \circ tile(m, k, transpose(B))
13
      ) \circ tile(n, k, A)
```



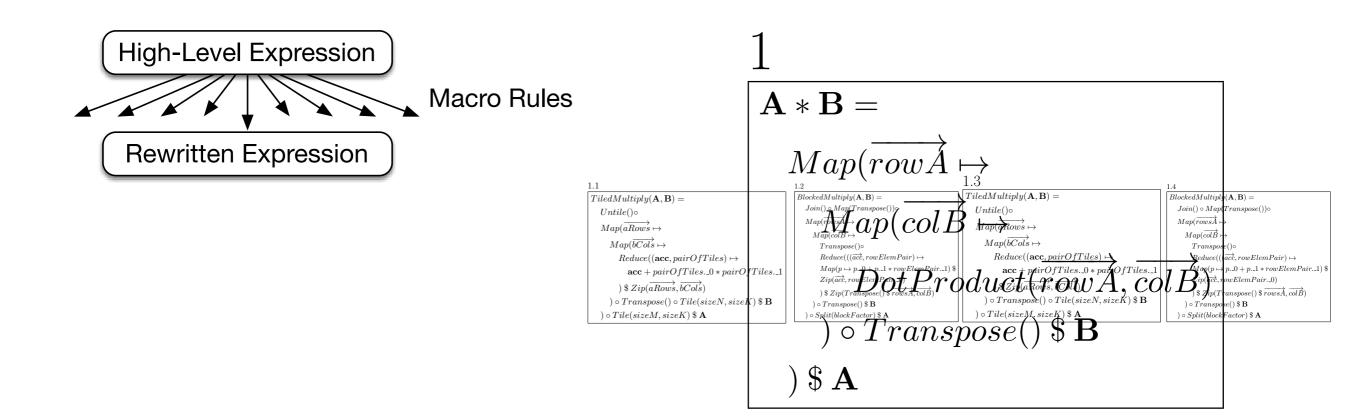
Apply blocking rules

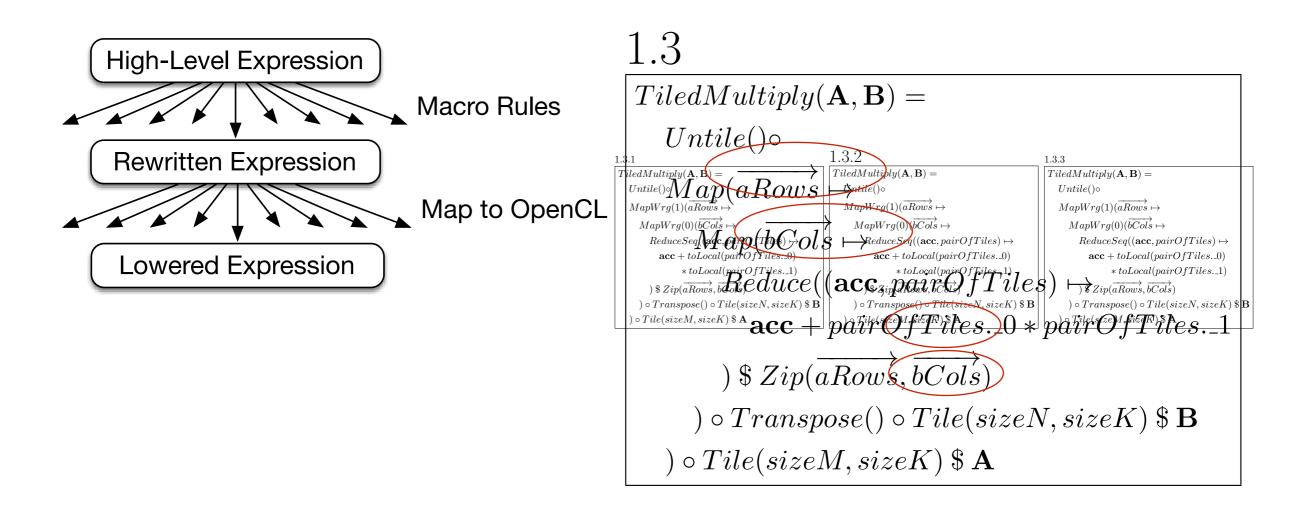


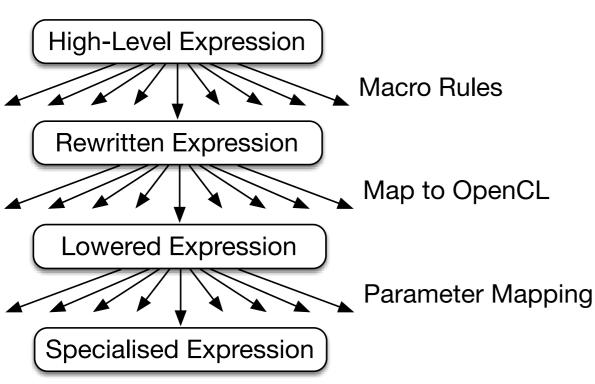


Register Blocking as a Rewrite Rules

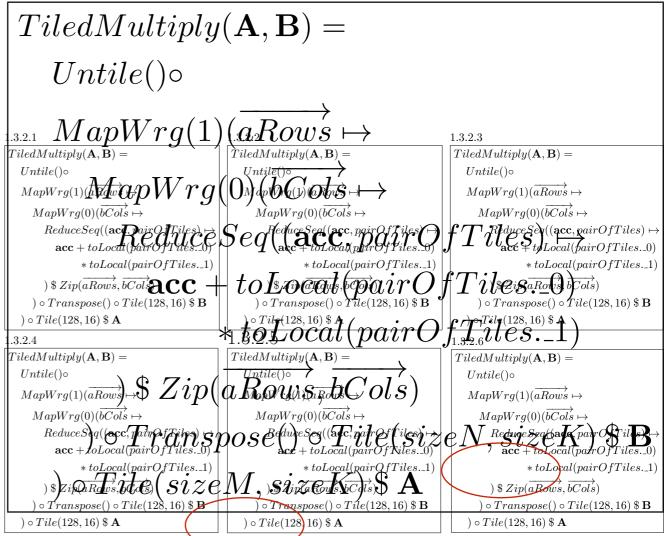
```
register Blocking =
    Map(f) \Rightarrow Join() \circ Map(Map(f)) \circ Split(k)
    Map(a \mapsto Map(b \mapsto f(a,b))) \Rightarrow Transpose() \circ Map(b \mapsto Map(a \mapsto f(a,b)))
    Map(f \circ g) \Rightarrow Map(f) \circ Map(g)
    Map(Reduce(f)) \Rightarrow Transpose() \circ Reduce((acc, x) \mapsto Map(f) \circ Zip(acc, x))
    Map(Map(f)) \Rightarrow Transpose() \circ Map(Map(f)) \circ Transpose()
    Transpose() \circ Transpose() \Rightarrow id
    Reduce(f) \circ Map(g) \Rightarrow Reduce((acc, x) \mapsto f(acc, g(x)))
    Map(f) \circ Map(g) \Rightarrow Map(f \circ g)
                                                                                                     В
                                                                               A
```

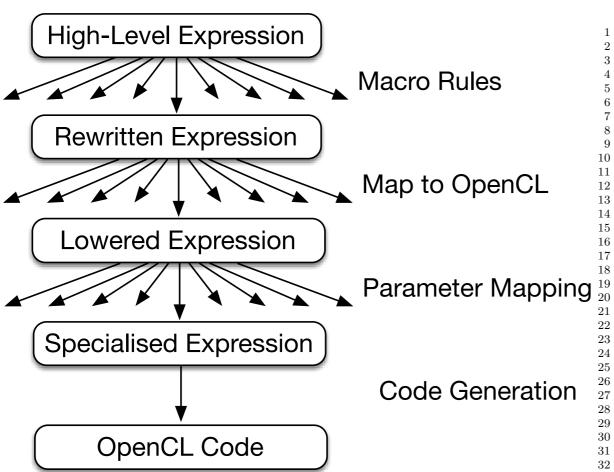






1.3.2





1.3.2.5

```
private float acq.0; private float blockOfA.0; ...; acc.31; private float blockOfA.0; ...; blockOfA.7;
                                                                      \begin{array}{c} \text{vstore4}(\text{vload4}(\text{lid1*M/4+2*i*M+16*w1+lid0,A}),\ 16*\text{lid1+lid0},\ \text{tileA});} \\ \text{vstore4}(\text{vload4}(\text{lid1*M/4+2*i*M+16*w1+lid0,A}),\ 16*\text{lid1+lid0},\ \text{tileA});} \\ \text{vstore4}(\text{vload4}(\text{lid1*M/4+2*i*M+16*w1+lid0,A}),\ 16*\text{lid1+lid0},\ \text{tileA});} \\ \text{barrier (...)}; \\ Red in Cerson in the property of the property 
                                                                                                     \begin{array}{l} \text{for (int } \texttt{j} = \texttt{0}; \texttt{j} < \texttt{8}; \texttt{j} + \texttt{H}) \ \{ \\ \texttt{blockOfA\_0} = \texttt{tileA} [\texttt{0} + \texttt{a} *\texttt{C} | \texttt{C} ! * \texttt{8}] + ... t \texttt{blockOfB\_0} \texttt{c} \texttt{tileA} [\texttt{p} *\texttt{p} *\texttt{p} ! \texttt{d} ! * \texttt{8}] \\ \texttt{blockOfB\_0} = \texttt{tileB} [\texttt{0} + \texttt{6} 4 *\texttt{j} + \texttt{lid0}]; \end{array} \\ \dots, t \texttt{blockOfB\_0} = \texttt{tileA} [\texttt{p} *\texttt{p} *\texttt{p} ! \texttt{d} ! \texttt{e} !
24
                                                                                                            acc_0 += blockOfA_0 * blockOfB_0; ...; acc_2s += blockOfA_7 * blockOfB_0; ...; acc_2s += blockOfA_0 * blockOfB_1 * ... to 19 to 000 to
                                                                                                              acc_3 += blockOfA_0 * blockOfB_3; ...; acc_31 += blockOfA_7 * blockOfB_3;
                                                                                                                                                                                                                                                                                                                          ) \ \ Zip(aRows,bCols)
30
                                                                                \begin{array}{c} C[\ 0+8*lid1*N+64*w0+64*w1*N+0*N+lid0] = acc.0; \ldots; C[\ 0+8*lid1*N+64*w0+64*w1*N+7*N+lid0] = acc.28; \\ C[16+8*lid1*N+04*w0+64*w1*N+0*N+lid0] = acc.29; \\ C[32+8*lid1*N+64*w0+64*w1*N+0*N+lid0] = acc.29; \ldots; C[32+8*lid1*N+64*w0+64*w1*N+7*N+lid0] = acc.30; \\ C[48+8*lid1*N+64*w0+64*w1*N+0*N+lid0] = acc.3; \ldots; C[48+8*lid1*N+64*w0+64*w1*N+7*N+lid0] = acc.31; \\ C[48+8*lid1*N+64*w0+64*w1*N+0*N+lid0] = acc.31; \\ C[48+8*lid1*N+64*w0+64*w1*N+7*N+lid0] = acc.31; \\ C[48+8*lid1*N+64*w0+64*w1*N+7*N+lid
                                                                                                                                                                                                         \circ Tile(128, 16) \$ A
```

Heuristics for Matrix Multiplication

For Macro Rules:

- Nesting depth
- Distance of addition and multiplication
- Number of times rules are applied

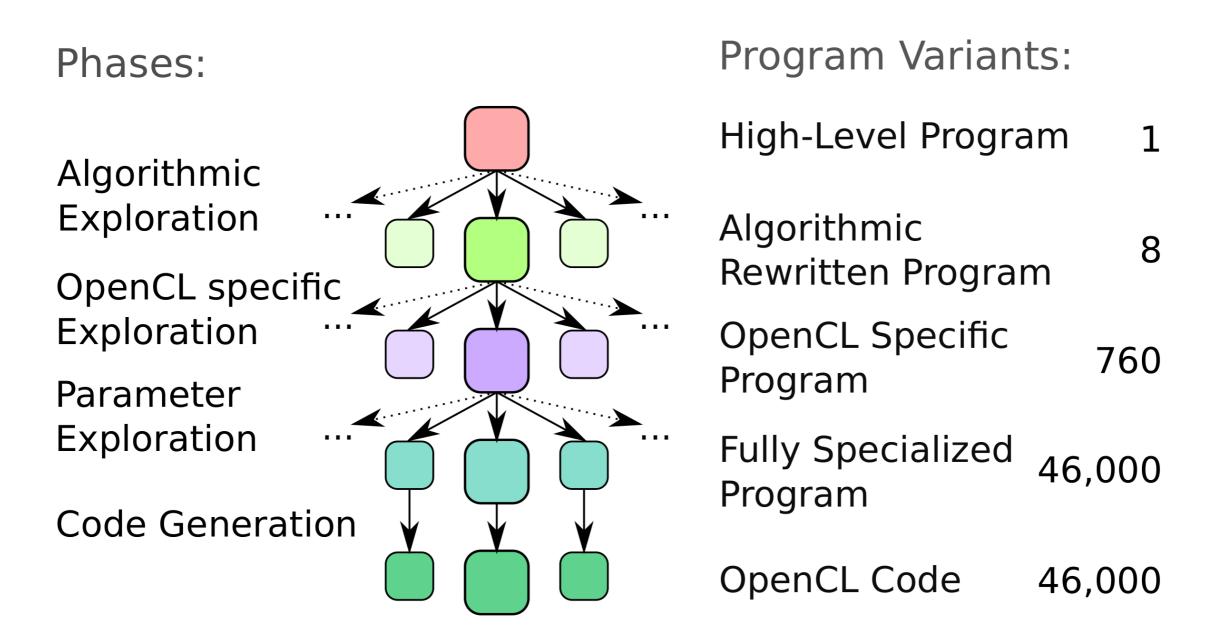
For Map to OpenCL:

- Fixed parallelism mapping
- Limited choices for mapping to local and global memory
- Follows best practice

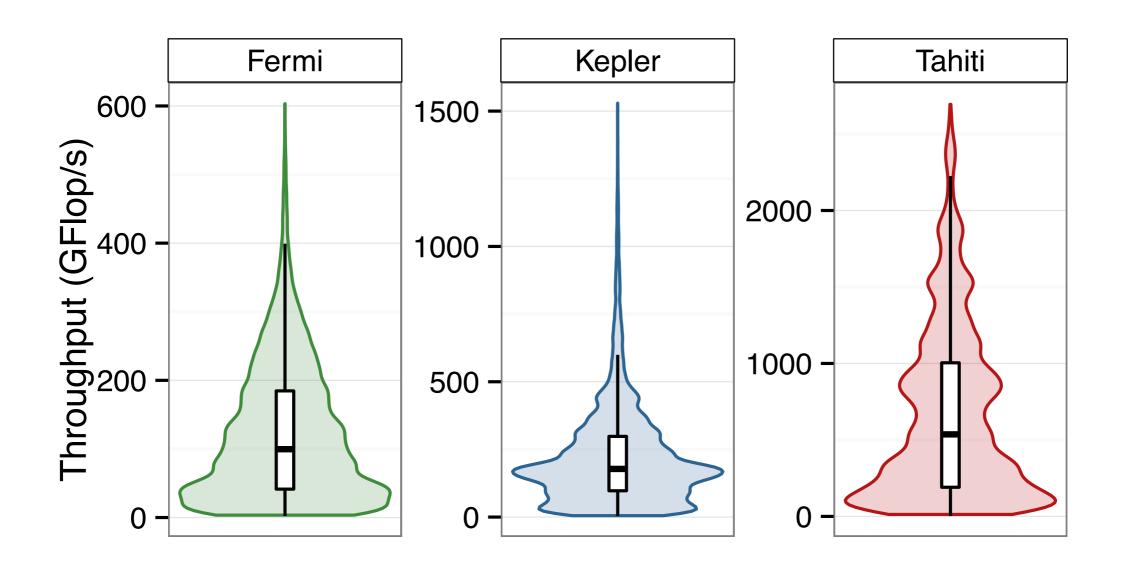
For Parameter Mapping:

- Amount of memory used
 - Global
 - Local
 - Registers
- Amount of parallelism
 - Work-items
 - Workgroup

Exploration in Numbers for Matrix Multiplication

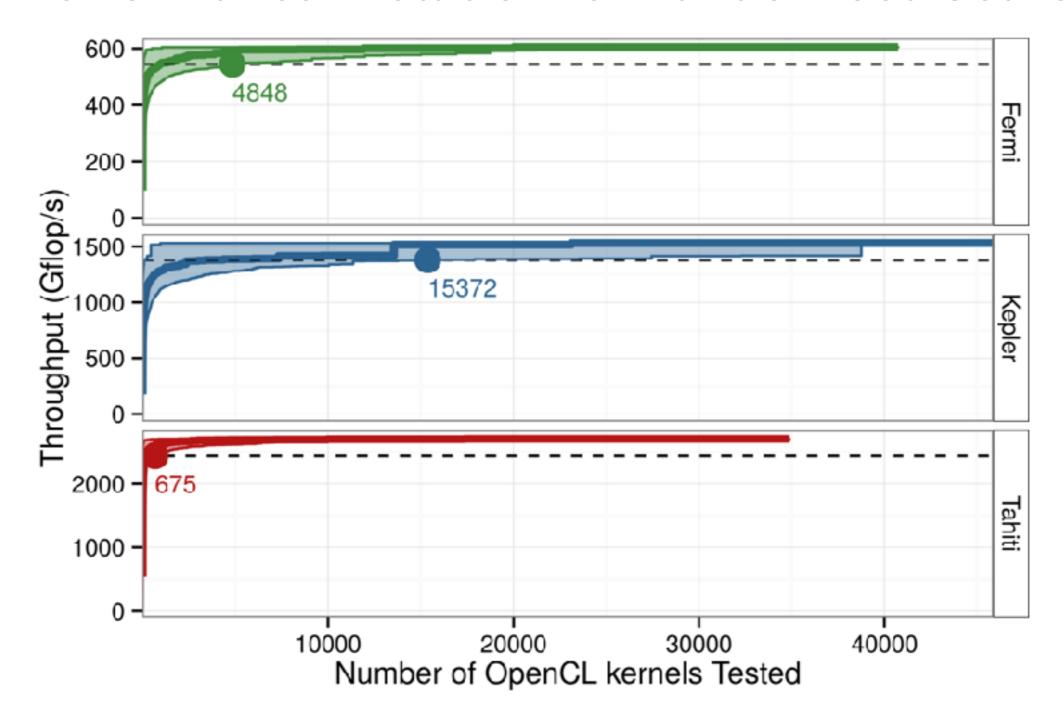


Exploration Space for Matrix Multiplication



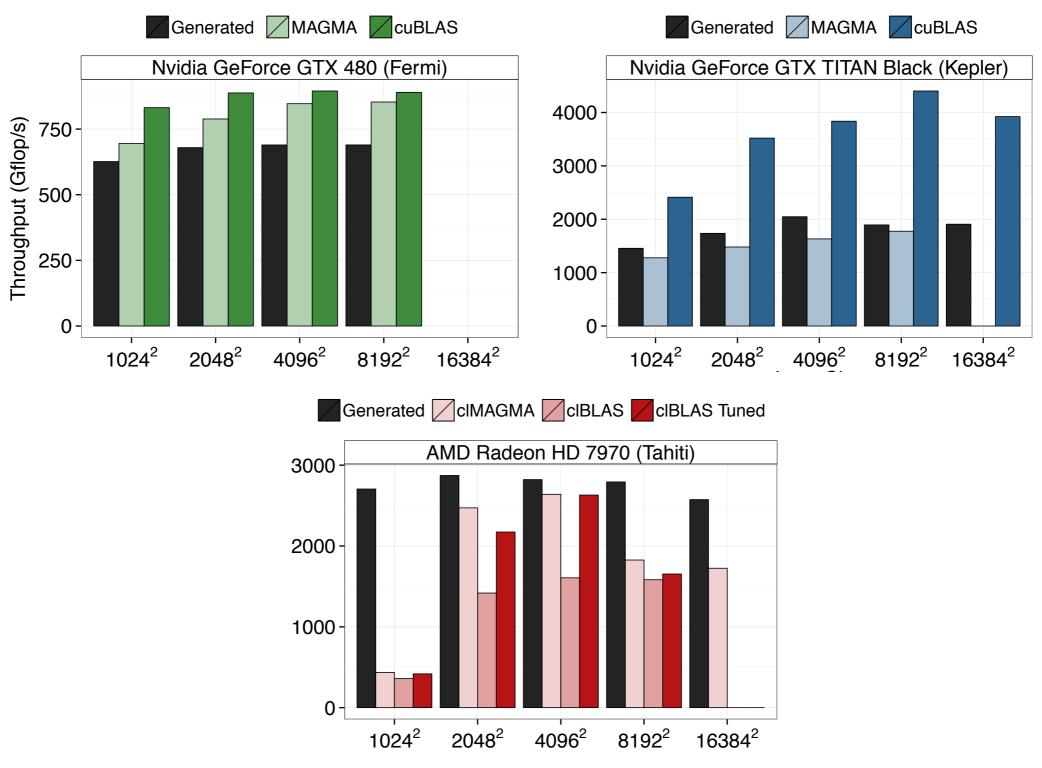
Only few OpenCL kernel with very good performance

Performance Evolution for Randomised Search



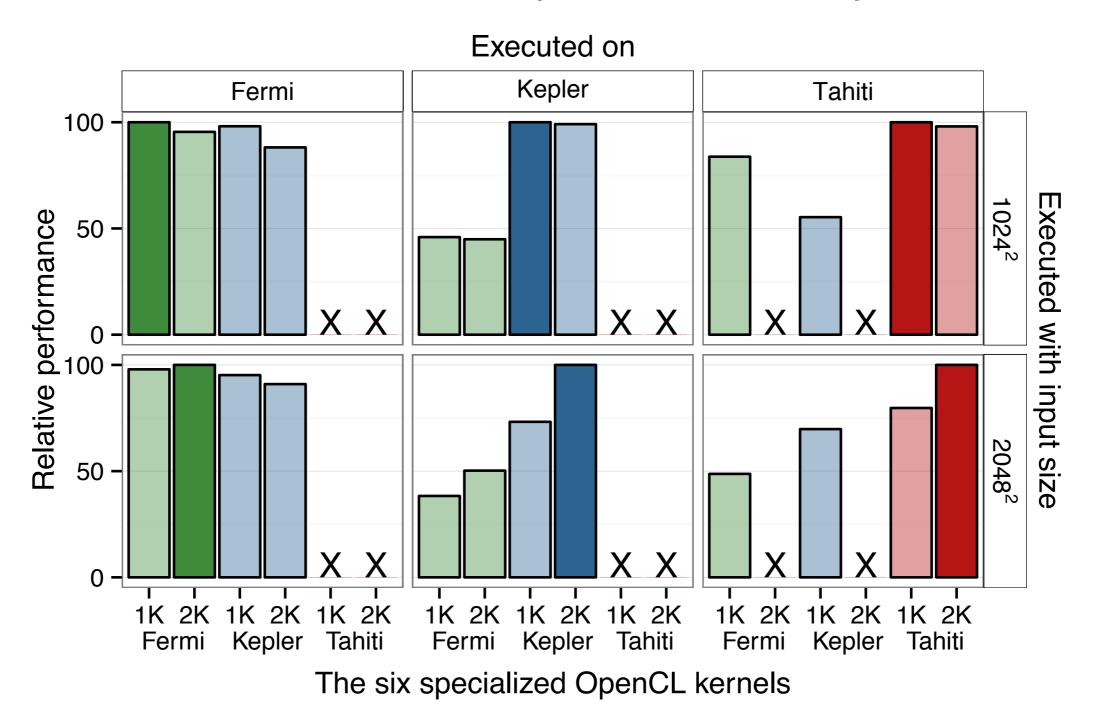
Even with a simple random search strategy one can expect to find a good performing kernel quickly

Performance Results Matrix Multiplication



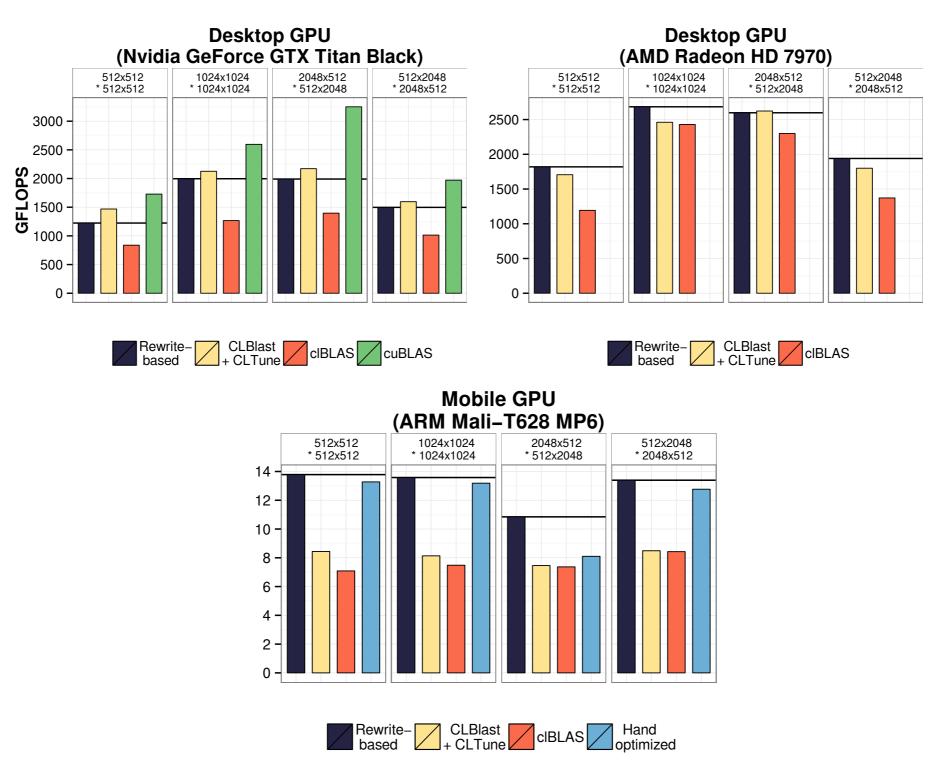
Performance close or better than hand-tuned MAGMA library

Performance Portability Matrix Multiplication



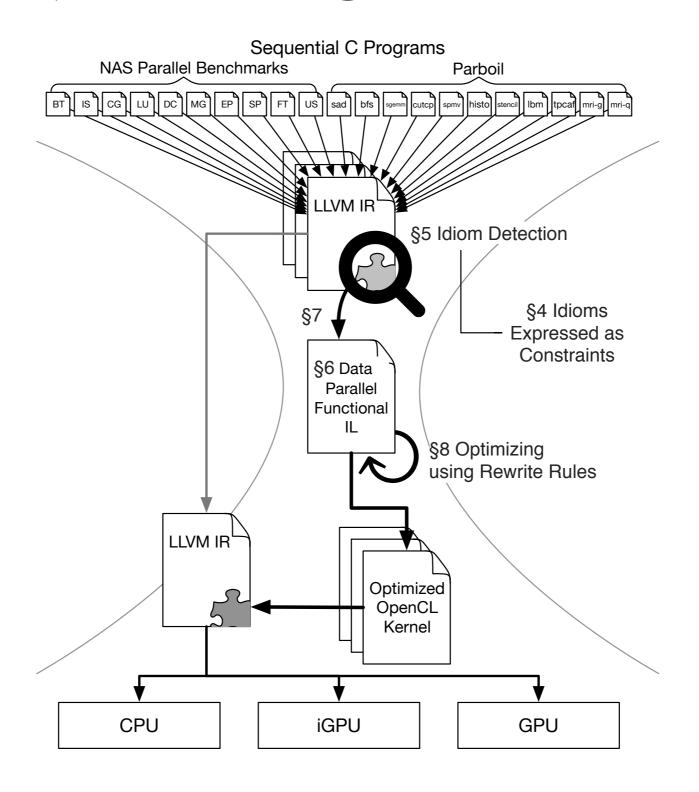
Generated kernels are specialised for device and input size

Desktop GPUs vs. Mobile GPU

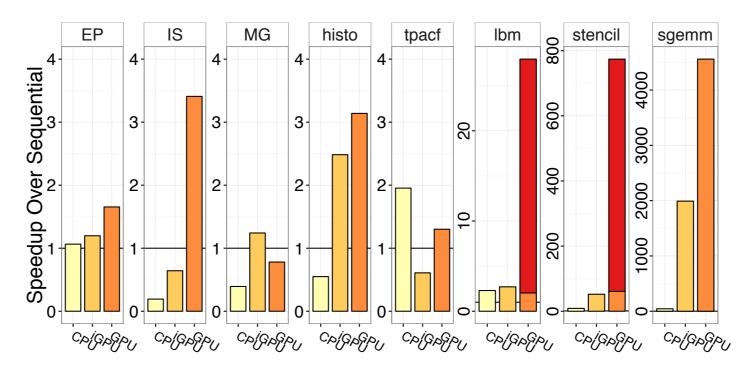


Performance portable even for mobile GPU device!

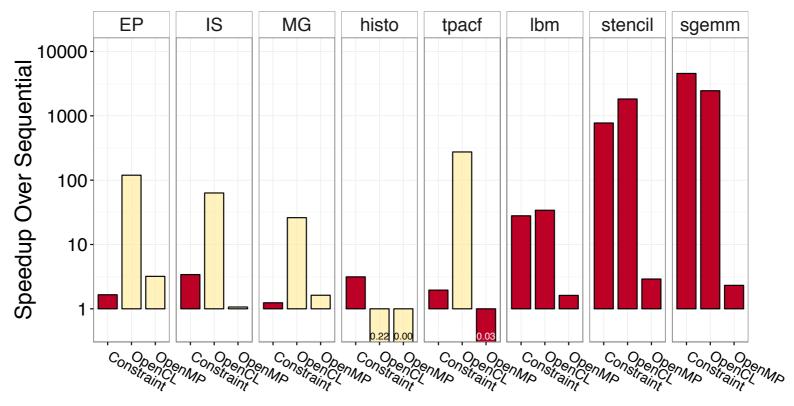
Using Lift as a code generation backend



Using Lift as a code generation backend



Heterogeneous code generation gives a speedup in all cases

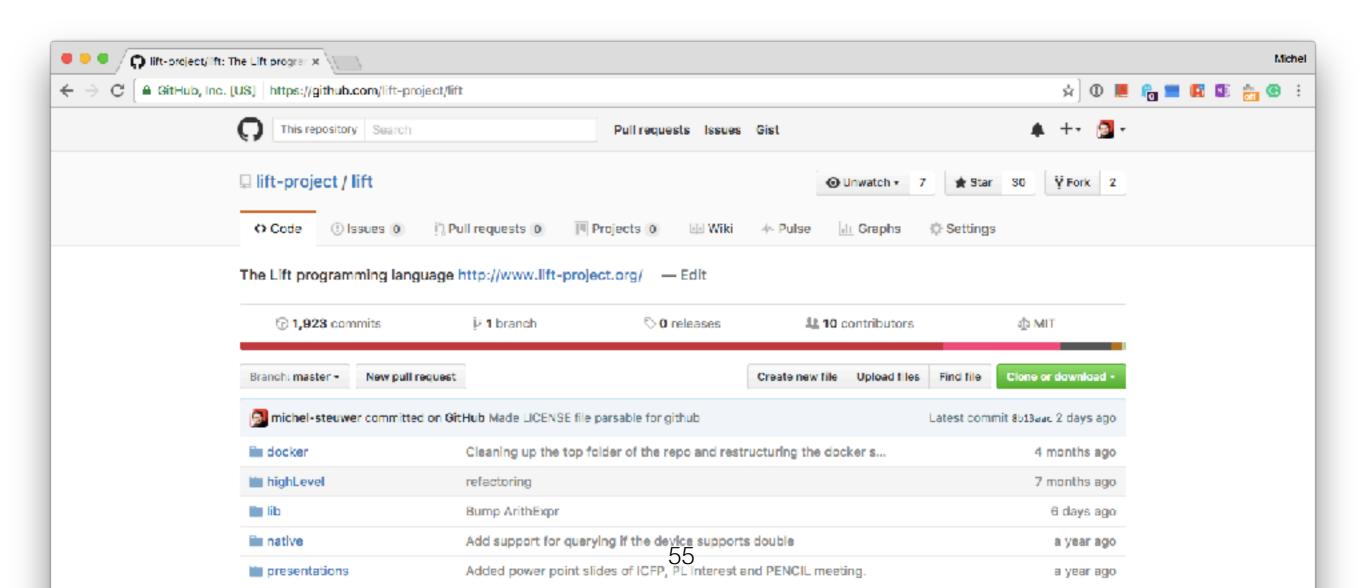


Performance close to manual written code —when parallelisation strategy is comparable

Lift is now Open-Source Software

http://www.lift-project.org/

https://github.com/lift-project/lift



The Lift Team



Christophe Dubach Lecturer University of Edinburgh



Michel Steuwer
Postdoc
University of Edinburgh



Toomas Remmelg
PhD Student
University of Edinburgh



Adam Harries
PhD Student
University of Edinburgh



Bastian Hagedorn
PhD Student
University of Münster



Larisa Stoltzfus
PhD Student
University of Edinburgh



Federico Pizzuti
PhD Student
University of Edinburgh



Naums Mogers
PhD Student
University of Edinburgh

The *Lift* Project: Performance Portable GPU Code Generation via Rewrite Rules

Michel Steuwer — <u>michel.steuwer@ed.ac.uk</u>

http://www.lift-project.org/



