







# THE UNIVERSITY of EDINBURGH INFORMATICS

- Largest Informatics Department in the UK:
  - > 500 academic and research staff
     + PhD students
- Overall 6 Research Institutes

  2 particular relevant for the topic of the talk:
- ICSA Institute for Computing Systems Architecture
  - Compiler & Architecture
  - Parallel Computing
  - •
- LFCS Laboratory for Foundations of Computer Science
  - Programming Languages and Foundations
  - Software Engineering
  - •

# Structured Parallel Programming

From High-Level Functional Expressions

to High-Performance OpenCL Code

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# The Problem(s)

- Parallel processors everywhere
- · Many different types: CPUs, GPUs, ...
- First Major Challenge:
   Parallel programming is hard.
   Optimising is even harder!
- Second Major Challenges:
   No portability of performance!









**Accelerator** 

**FPGA** 





# Part I: Addressing the Programmability Challenge



Case Study: Parallel reduction in OpenCL



Case Study: Parallel reduction in OpenCL

**Kernel** function executed in parallel by multiple work-items

Work-items are identified by a unique global id



Case Study: Parallel reduction in OpenCL

Work-items are grouped into work-groups

Local id within work-group



Case Study: Parallel reduction in OpenCL

Big, but slow **global** memory

Small, but fast local memory

```
kernel void reduce(global)float* g_idata,(global) float* g_odata,
                   unsigned int n, local float* l_data) {
  unsigned int tid = get local id(0);
  unsigned int i
                   = get_global_id(0);
  l data[tid] = (i < n) ? g idata[i] : 0;
  barrier(CLK_LOCAL_MEM_FENCE);
  // do reduction in local memory
  for (unsigned int s=1; s < get local size(0); s*= 2) {</pre>
   if ((tid % (2*s)) == 0) {
      l data[tid] += l data[tid + s];
     barrier(CLK_LOCAL_MEM_FENCE);
    write result for this work-group to global memory
  if (tid == 0) g odata[get group id(0)] = l data[0];
```

Memory **barriers** for consistency



Case Study: Parallel reduction in OpenCL

Functionally correct implementations in OpenCL are hard!



#### The SkelCL Programming Model

#### Three high-level features added to OpenCL:

parallel container data types
 for unified memory management between CPU and (multiple) GPUs

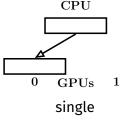
- implicit memory transfers between CPU and GPU
- lazy copying minimizes data transfers
- recurring patterns of parallelism

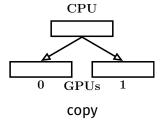
(a.k.a., algorithmic skeletons) for easily expressing parallel computation patterns;

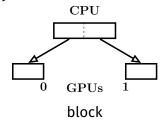
$$zip \ (\oplus) \ [x_1, ..., x_n] \ [y_1, ..., y_n] = [x_1 \oplus y_1, ..., x_n \oplus y_n]$$
  
reduce  $(\oplus) \ \oplus_{id} \ [x_1, ..., x_n] = \oplus_{id} \oplus x_1 \oplus ... \oplus x_n$ 

data distribution and redistribution

mechanisms for transparent data transfers in multi-GPU systems.









#### The SkelCL Library by Example

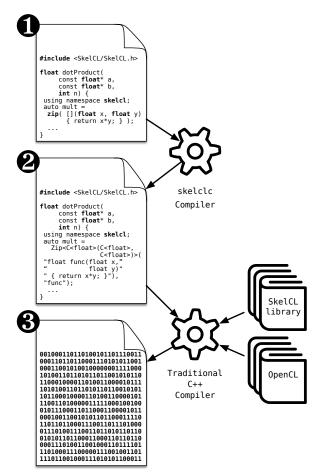
 $dotProduct A B = reduce (+) 0 \circ zip (x) A B$ 

```
#include <SkelCL/SkelCL.h>
#include <SkelCL/Zip.h>
#include <SkelCL/Reduce.h>
#include <SkelCL/Vector.h>
float dotProduct(const float* a, const float* b, int n) {
  using namespace skelcl;
  skelcl::init( 1_device.type(deviceType::ANY) );
 auto mult = zip([](float x, float y) { return x*y; });
 auto sum = reduce([](float x, float y) { return x+y; }, 0);
 Vector<float> A(a, a+n); Vector<float> B(b, b+n);
 Vector<float> C = sum( mult(A, B) );
  return C.front();
```



#### From SkelCL to OpenCL

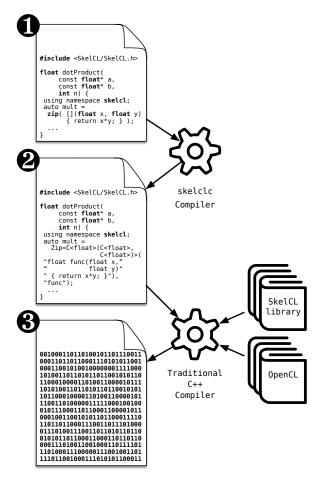
```
#include <SkelCL/SkelCL.h>
#include <SkelCL/Zip.h>
#include <SkelCL/Reduce.h>
#include <SkelCL/Vector.h>
float dotProduct(const float* a, const float* b, int n) {
 using namespace skelcl;
  skelcl::init( 1 device.type(deviceType::ANY) );
               zip([](float x, float y) { return x*y; });
  auto mult =
 auto sum = reduce([](float x, float y) { return x+y; }, 0);
 Vector<float> A(a, a+n); Vector<float> B(b, b+n);
 Vector<float> C = sum( mult(A, B) );
 return C.front();
```





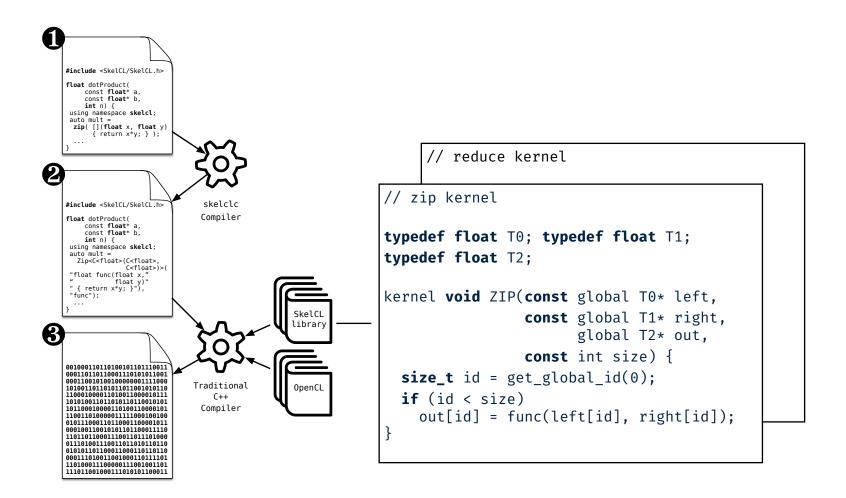
#### From SkelCL to OpenCL

```
#include <SkelCL/SkelCL.h>
#include <SkelCL/Zip.h>
#include <SkelCL/Reduce.h>
#include <SkelCL/Vector.h>
float dotProduct(const float* a, const float* b, int n) {
 using namespace skelcl:
  skelcl::init( 1 device.type(deviceType::ANY) );
 auto mult = Zip<Container<float>(Container<float>,
                                   Container<float>)>(
  Source("float func(float x, float y) {return x*y;}"));
 auto sum = Reduce<Vector<float>(Vector<float>)>(
  Source("float func(float x, float y) {return x+y;}"), "0");
 Vector<float> A(a, a+n); Vector<float> B(b, b+n);
 Vector<float> C = sum( mult(A, B) );
 return C.front();
```





#### From SkelCL to OpenCL





#### Two Novel Algorithmic Skeletons

#### **Stencil Computations**

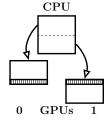
Example: Gaussian blur





gauss  $M = \text{stencil f 1 } \overline{0} M$ where f is the weighted gaussian kernel

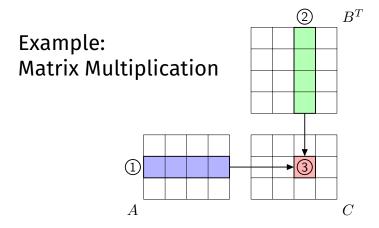
Multi-GPU support:



overlap distribution



#### **Allpairs Computations**



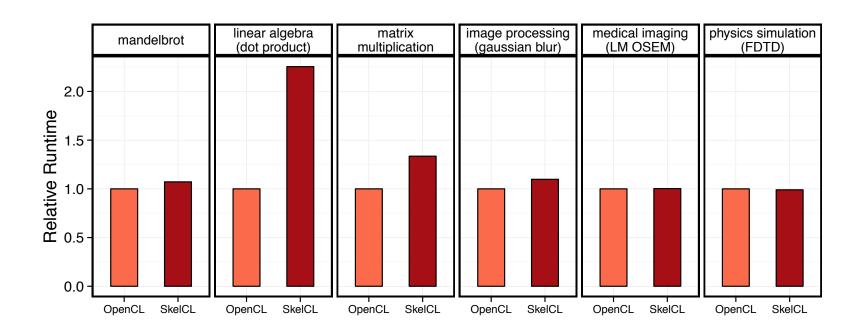
 $A \times B = allpairs dotProduct A B^T$ 

Optimization for zipReduce patterns:

 $dotProduct \ a \ b = zipReduce \ (+) \ 0 \ (x) \ a \ b$ 

Multi-GPU support with **block** and **copy** distribution

#### SkelCL Evaluation — Performance

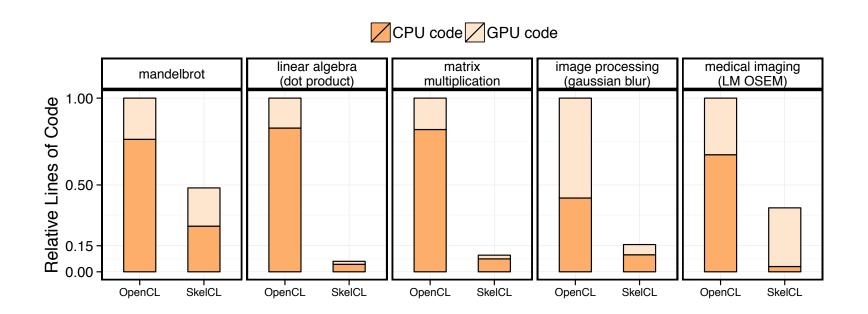


#### SkelCL performance close to native OpenCL code!

(Exception: dot product ... wait for Part II)



#### SkelCL Evaluation — Productivity



SkelCL programs are significantly shorter!

SkelCL is open source software and available from <a href="http://github.com/skelcl/skelcl">http://github.com/skelcl/skelcl</a>

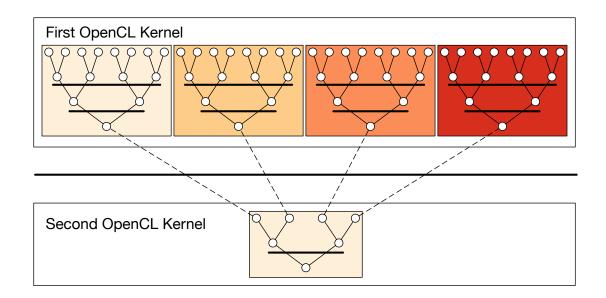


# Part II: Addressing the Performance Portability Challenge



# Case Study: Parallel Reduction in OpenCL

- Summing up all values of an array
- Comparison of 7 implementations by Nvidia
- Investigating complexity and efficiency of optimisations





#### **Unoptimised Implementation Parallel Reduction**

```
kernel void reduceO(global float* g_idata, global float* g_odata,
                    unsigned int n, local float* l data) {
 unsigned int tid = get_local_id(0);
 unsigned int i = get_global_id(0);
 l data[tid] = (i < n) ? g idata[i] : 0;</pre>
 barrier(CLK_LOCAL_MEM_FENCE);
 // do reduction in local memory
 for (unsigned int s=1; s < get_local_size(0); s*= 2) {</pre>
   if ((tid % (2*s)) == 0) {
      l data[tid] += l data[tid + s];
      barrier(CLK_LOCAL_MEM_FENCE);
 // write result for this work-group to global memory
  if (tid == 0) g_odata[get_group_id(0)] = l_data[0];
```



# **Avoid Divergent Branching**

```
kernel void reduce1(global float* g_idata, global float* g_odata,
                    unsigned int n, local float* l_data) {
 unsigned int tid = get_local_id(0);
  unsigned int i = get_global_id(0);
 l data[tid] = (i < n) ? g idata[i] : 0;</pre>
  barrier(CLK_LOCAL_MEM_FENCE);
 for (unsigned int s=1; s < get_local_size(0); s*= 2) {</pre>
    // continuous work-items remain active
    int index = 2 * s * tid;
    if (index < get_local_size(0)) {</pre>
     l_data[index] += l_data[index + s];
    barrier(CLK LOCAL MEM FENCE);
 if (tid == 0) g_odata[get_group_id(0)] = l_data[0];
```



# **Avoid Interleaved Addressing**

```
kernel void reduce2(global float* g_idata, global float* g_odata,
                    unsigned int n, local float* l data) {
 unsigned int tid = get local id(0);
  unsigned int i = get global id(0);
 l data[tid] = (i < n) ? g idata[i] : 0;</pre>
  barrier(CLK_LOCAL_MEM_FENCE);
 // process elements in different order
 // requires commutativity
 for (unsigned int s=get_local_size(0)/2; s>0; s>>=1) {
    if (tid < s) {
     l_data[tid] += l_data[tid + s];
    barrier(CLK LOCAL MEM FENCE);
  if (tid == 0) g_odata[get_group_id(0)] = l_data[0];
```



#### Increase Computational Intensity per Work-Item

```
kernel void reduce3(global float* g_idata, global float* g_odata,
                    unsigned int n, local float* l data) {
  unsigned int tid = get_local_id(0);
  unsigned int i = get_group_id(0) * (get_local_size(0)*2)
                                    + get local id(0);
  l_data[tid] = (i < n) ? g_idata[i] : 0;</pre>
  // performs first addition during loading
  if (i + get local size(0) < n)</pre>
   l_data[tid] += g_idata[i+get_local_size(0)];
  barrier(CLK_LOCAL_MEM_FENCE);
  for (unsigned int s=get local size(0)/2; s>0; s>>=1) {
    if (tid < s) {
      l_data[tid] += l_data[tid + s];
    barrier(CLK LOCAL MEM FENCE);
  if (tid == 0) g_odata[get_group_id(0)] = l_data[0];
```



# **Avoid Synchronisation inside a Warp**

```
kernel void reduce4(global float* g idata, global float* g odata,
                    unsigned int n, local volatile float* l_data) {
  unsigned int tid = get_local_id(0);
  unsigned int i = get_group_id(0) * (get_local_size(0)*2)
                                    + get local id(0);
  l_data[tid] = (i < n) ? g_idata[i] : 0;</pre>
  if (i + get_local_size(0) < n)</pre>
    l_data[tid] += g_idata[i+get_local_size(0)];
  barrier(CLK_LOCAL_MEM_FENCE);
  # pragma unroll 1
  for (unsigned int s=get_local_size(0)/2; s>32; s>>=1) {
    if (tid < s) { l_data[tid] += l_data[tid + s]; }</pre>
    barrier(CLK LOCAL MEM FENCE); }
  // this is not portable OpenCL code!
  if (tid < 32) {
    if (WG_SIZE >= 64) { l_data[tid] += l_data[tid+32]; }
    if (WG SIZE >= 32) { l data[tid] += l data[tid+16]; }
    if (WG_SIZE >= 16) { l_data[tid] += l_data[tid+ 8]; }
    if (WG_SIZE >= 8) { l_data[tid] += l_data[tid+ 4]; }
    if (WG_SIZE >= 4) { l_data[tid] += l_data[tid+ 2]; }
    if (WG_SIZE >= 2) { l_data[tid] += l_data[tid+ 1]; } }
  if (tid == 0) g odata[get group id(0)] = l data[0]; }
```

# **Complete Loop Unrolling**

```
kernel void reduce5(global float* g_idata, global float* g_odata,
                    unsigned int n, local volatile float* l_data) {
  unsigned int tid = get_local_id(0);
  unsigned int i = get_group_id(0) * (get_local_size(0)*2)
                                    + get local id(0);
 l_data[tid] = (i < n) ? g_idata[i] : 0;</pre>
  if (i + get_local_size(0) < n)</pre>
    l_data[tid] += g_idata[i+get_local_size(0)];
  barrier(CLK_LOCAL_MEM_FENCE);
  if (WG_SIZE >= 256) {
    if (tid < 128) { l_data[tid] += l_data[tid+128]; }</pre>
    barrier(CLK_LOCAL_MEM_FENCE); }
  if (WG SIZE >= 128) {
    if (tid < 64) { l_data[tid] += l_data[tid+ 64]; }</pre>
    barrier(CLK_LOCAL_MEM_FENCE); }
  if (tid < 32) {
    if (WG_SIZE >= 64) { l_data[tid] += l_data[tid+32]; }
    if (WG_SIZE >= 32) { l_data[tid] += l_data[tid+16]; }
    if (WG_SIZE >= 16) { l_data[tid] += l_data[tid+ 8]; }
    if (WG_SIZE >= 8) { l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) { l data[tid] += l data[tid+ 2]; }
    if (WG SIZE >= 2) { l data[tid] += l data[tid+ 1]; } }
  if (tid == 0) g_odata[get_group_id(0)] = l_data[0]; }
```

# **Fully Optimised Implementation**

```
kernel void reduce6(global float* g_idata, global float* g_odata,
                    unsigned int n, local volatile float* l data) {
  unsigned int tid = get_local_id(0);
  unsigned int i = get_group_id(0) * (get_local_size(0)*2)
                                   + get_local_id(0);
  unsigned int gridSize = WG SIZE * get num groups(0);
 l data[tid] = 0;
  while (i < n) { l data[tid] += g idata[i];</pre>
                  if (i + WG SIZE < n)</pre>
                    l_data[tid] += g_idata[i+WG_SIZE];
                  i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
  if (WG SIZE >= 256) {
    if (tid < 128) { l_data[tid] += l_data[tid+128]; }</pre>
    barrier(CLK LOCAL MEM FENCE); }
  if (WG SIZE >= 128) {
    if (tid < 64) { l data[tid] += l data[tid+ 64]; }
    barrier(CLK_LOCAL_MEM_FENCE); }
  if (tid < 32) {
    if (WG SIZE >= 64) { l data[tid] += l data[tid+32]; }
   if (WG_SIZE >= 32) { l_data[tid] += l_data[tid+16]; }
    if (WG SIZE >= 16) { l data[tid] += l data[tid+ 8]; }
    if (WG SIZE >= 8) { l data[tid] += l data[tid+ 4]; }
    if (WG SIZE >= 4) { l data[tid] += l data[tid+ 2]; }
    if (WG SIZE >= 2) { l data[tid] += l data[tid+ 1]; } }
  if (tid == 0) g odata[get group id(0)] = l data[0]; }
```

# **Case Study Conclusions**

- Optimising OpenCL is complex
  - Understanding of target hardware required
- Program changes not obvious
- Is it worth it? ...

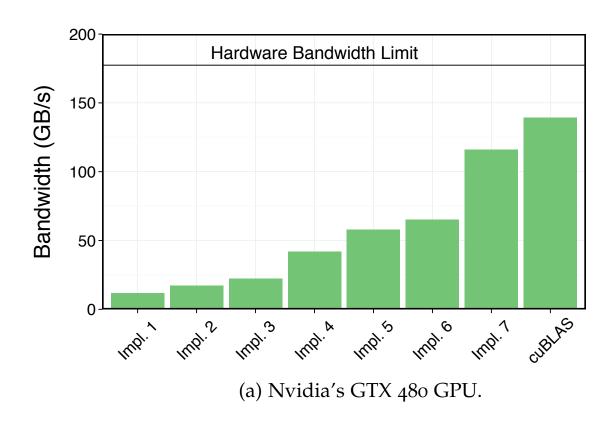
```
kernel
void reduce0(global float* g idata,
             global float* g_odata,
             unsigned int n,
             local float* l data) {
 unsigned int tid = get local id(0);
  unsigned int i = get_global_id(0);
 l data[tid] = (i < n) ? g idata[i] : 0;</pre>
  barrier(CLK LOCAL MEM FENCE);
  for (unsigned int s=1;
       s < get local size(0); s*= 2) {
    if ((tid \% (2*s)) == 0) {
      l data[tid] += l data[tid + s];
    barrier(CLK_LOCAL_MEM_FENCE);
 if (tid == 0)
    g_odata[get_group_id(0)] = l_data[0];
```

**Unoptimized Implementation** 

```
kernel
void reduce6(global float* g idata,
             global float* g odata,
             unsigned int n,
             local volatile float* l data) {
 unsigned int tid = get local id(0);
 unsigned int i =
   get_group_id(0) * (get_local_size(0)*2)
                    + get_local_id(0);
 unsigned int gridSize =
   WG SIZE * get num groups(0);
 l_data[tid] = 0;
  while (i < n) {
   l_data[tid] += g_idata[i];
   if (i + WG SIZE < n)</pre>
     l data[tid] += g idata[i+WG SIZE];
    i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
 if (WG SIZE >= 256) {
    if (tid < 128) {
     l_data[tid] += l_data[tid+128]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
 if (WG_SIZE >= 128) {
    if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
    barrier(CLK_LOCAL_MEM_FENCE); }
 if (tid < 32) {
    if (WG SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
    if (WG SIZE >= 32) {
     l data[tid] += l data[tid+16]; }
    if (WG SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
     l_data[tid] += l_data[tid+ 4]; }
   if (WG SIZE >= 4) {
     l data[tid] += l data[tid+ 2]; }
    if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
 if (tid == 0)
   g_odata[get_group_id(0)] = l_data[0];
```

**Fully Optimized Implementation** 

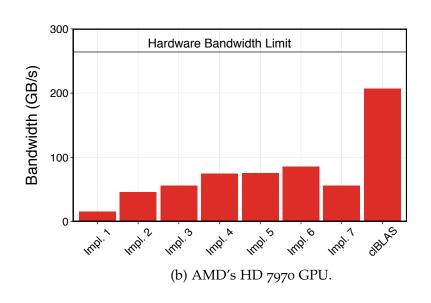
#### **Performance Results Nvidia**

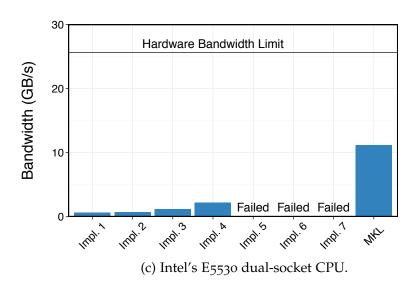


- ... Yes! Optimising improves performance by a factor of 10!
- Optimising is important, but ...



#### Performance Results AMD and Intel

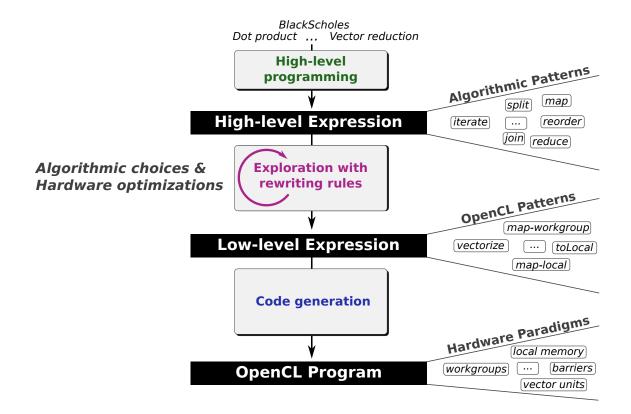




- ... unfortunately, optimisations in OpenCL are not portable!
- Challenge: how to achieving portable performance?



# Generating Performance Portable Code using Rewrite Rules



Ambition: automatic generation of Performance Portable code



# Walkthrough

rewrite rules

code generation



```
vecSum = reduce o join o map-workgroup (
    join o toGlobal (map-local (map-seq id)) o split 1 o
    join o map-warp (
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 1 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 2 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 4 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 8 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 16 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 32
        ) o split 64 o
        join o map-local (reduce-seq (+) 0) o split 2 o reorder-stride 64 o
        join o toLocal (map-local (reduce-seq (+) 0)) o
        split (blockSize/128) o reorder-stride 128
        ) o split blockSize
```

```
kernel
void reduce6(global float* g idata,
             global float* g odata,
             unsigned int n,
             local volatile float* l_data) {
 unsigned int tid = get local id(0);
 unsigned int i =
   get_group_id(0) * (get_local_size(0)*2)
                    + get_local_id(0);
  unsigned int gridSize =
   WG SIZE * get num groups(0);
 l_data[tid] = 0;
  while (i < n) {
    l_data[tid] += g_idata[i];
    if (i + WG SIZE < n)</pre>
     l_data[tid] += g_idata[i+WG_SIZE];
    i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
  if (WG SIZE >= 256) {
    if (tid < 128) {
     l_data[tid] += l_data[tid+128]; }
    barrier(CLK_LOCAL_MEM_FENCE); }
 if (WG_SIZE >= 128) {
    if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
    barrier(CLK_LOCAL_MEM_FENCE); }
 if (tid < 32) {
    if (WG_SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
    if (WG SIZE >= 32) {
     l data[tid] += l data[tid+16]; }
    if (WG SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
      l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) {
     l data[tid] += l data[tid+ 2]; }
    if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
 if (tid == 0)
   g_odata[get_group_id(0)] = l_data[0];
```

#### Walkthrough

sum(vec) = reduce(+, 0, vec)

rewrite rules code generation

```
join ∘ toGlobal (map-local (map-seg id)) ∘ split 1 ∘
  join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 1 ∘
  join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 2 ∘
  join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 4 ∘
  join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 8 ∘
  join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 16 ∘
  join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 32
) o split 64 o
join ∘ map-local (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 64 ∘
split (blockSize/128) o reorder-stride 128
```

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```

```
kernel
void reduce6(global float* g idata,
             global float* g odata,
             unsigned int n,
             local volatile float* l data) {
 unsigned int tid = get local id(0);
 unsigned int i =
   get_group_id(0) * (get_local_size(0)*2)
                    + get_local_id(0);
 unsigned int gridSize =
   WG_SIZE * get_num_groups(0);
 l_data[tid] = 0;
 while (i < n) {
    l_data[tid] += g_idata[i];
   if (i + WG SIZE < n)</pre>
      l data[tid] += g idata[i+WG SIZE];
   i += gridSize; }
  barrier(CLK LOCAL MEM FENCE);
 if (WG SIZE >= 256) {
    if (tid < 128) {
      l data[tid] += l data[tid+128]; }
    barrier(CLK_LOCAL_MEM_FENCE); }
 if (WG_SIZE >= 128) {
    if (tid < 64) {
      l data[tid] += l data[tid+ 64]; }
    barrier(CLK_LOCAL_MEM_FENCE); }
 if (tid < 32) {
    if (WG SIZE >= 64) {
      l_data[tid] += l_data[tid+32]; }
   if (WG_SIZE >= 32) {
      l data[tid] += l data[tid+16]; }
   if (WG SIZE >= 16) {
      l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
      l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) {
      l data[tid] += l data[tid+ 2]; }
    if (WG SIZE >= 2) {
      l_data[tid] += l_data[tid+ 1]; } }
 if (tid == 0)
    g_odata[get_group_id(0)] = l_data[0];
```

# 1 Algorithmic Primitives (a.k.a. algorithmic skeletons)

map(f, x):  $|f(x_1)|f(x_2)|f(x_3)|f(x_4)|f(x_5)|f(x_6)|f(x_7)|f(x_8)$  $x_1 | x_2 | x_3 | x_4 | x_5 | x_6 | x_7 | x_8 |$ zip(x, y):  $\Rightarrow (x_1, y_1)(x_2, y_2)(x_3, y_3)(x_4, y_4)(x_5, y_5)(x_6, y_6)(x_7, y_7)(x_8, y_8)$  $y_1 | y_2 | y_3 | y_4 | y_5 | y_6 | y_7 | y_8$ reduce(+, 0, x):  $\begin{vmatrix} x_1 & x_2 & x_3 & x_4 & x_5 & x_6 & x_7 & x_8 \end{vmatrix}$  $x_1 + x_2 + x_3 + x_4 + x_5 + x_6 + x_7 + x_8$ split(n, x):  $\begin{bmatrix} x_2 & x_3 & x_4 & x_5 & x_6 & x_7 & x_8 \end{bmatrix}$ join(x):  $x_5 x_6$  $x_1 | x_2 | x_3 | x_4 | x_5 | x_6 | x_7 | x_8$ iterate(f, n, x):  $\longmapsto f( \dots f( x_1 x_2 x_3 x_4 x_5 x_6 x_7 x_8 ) \dots )$  $\begin{vmatrix} x_1 & x_2 & x_3 & x_4 & x_5 & x_6 & x_7 & x_8 \end{vmatrix}$ reorder( $\sigma$ , x):  $\begin{vmatrix} x_{\sigma(1)} | x_{\sigma(2)} | x_{\sigma(3)} | x_{\sigma(4)} | x_{\sigma(5)} | x_{\sigma(6)} | x_{\sigma(7)} | x_{\sigma(8)}$  $x_1 \mid x_2 \mid x_3 \mid x_4 \mid x_5 \mid x_6 \mid x_7 \mid x_8 \mid$ 

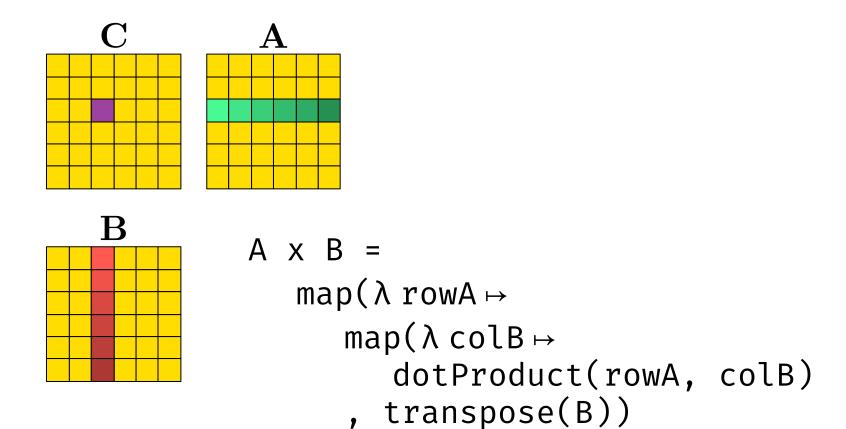


# **1** High-Level Programs

```
scal(a, vec) = map(\lambda x \mapsto x*a, vec)
asum(vec) = reduce(+, 0, map(abs, vec))
dotProduct(x, y) = reduce(+, 0, map(*, zip(x, y)))
gemv(mat, x, y, \alpha, \beta) =
   map(+, zip(
       map(\lambda row \rightarrow scal(\alpha, dotProduct(row, x)), mat),
       scal(\beta, y))
```



# **1** High-Level Programs





, A)

#### Walkthrough

rewrite rules

code generation

```
2
```

```
vecSum = reduce o join o map-workgroup (
    join o toGlobal (map-local (map-seq id)) o split 1 o
    join o map-warp (
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 1 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 2 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 4 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 8 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 16 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 32
        ) o split 64 o
        join o map-local (reduce-seq (+) 0) o split 2 o reorder-stride 64 o
        join o toLocal (map-local (reduce-seq (+) 0)) o
        split (blockSize/128) o reorder-stride 128
        ) o split blockSize
```

```
kernel
void reduce6(global float* g idata,
             global float* g odata,
             unsigned int n,
             local volatile float* l_data) {
 unsigned int tid = get local id(0);
 unsigned int i =
   get_group_id(0) * (get_local_size(0)*2)
                    + get_local_id(0);
  unsigned int gridSize =
   WG SIZE * get num groups(0);
 l_data[tid] = 0;
  while (i < n) {
    l_data[tid] += g_idata[i];
    if (i + WG SIZE < n)</pre>
     l_data[tid] += g_idata[i+WG_SIZE];
    i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
  if (WG SIZE >= 256) {
    if (tid < 128) {
     l_data[tid] += l_data[tid+128]; }
    barrier(CLK_LOCAL_MEM_FENCE); }
 if (WG_SIZE >= 128) {
    if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
    barrier(CLK_LOCAL_MEM_FENCE); }
 if (tid < 32) {
    if (WG_SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
    if (WG SIZE >= 32) {
     l data[tid] += l data[tid+16]; }
    if (WG SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
      l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) {
     l data[tid] += l data[tid+ 2]; }
    if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
 if (tid == 0)
    g_odata[get_group_id(0)] = l_data[0];
```

#### Walkthrough

 $1) \quad sum(vec) = reduce(+, 0, vec)$ 

rewrite rules

code generation

kernel

```
2
```

```
vecSum = reduce ∘ join ∘ map-workgroup (
    join ∘ toGlobal (map-local (map-seq id)) ∘ split 1 ∘
    join ∘ map-warp (
        join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 1 ∘
        join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 2 ∘
        join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 4 ∘
        join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 8 ∘
        join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 16 ∘
        join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 32
    ) ∘ split 64 ∘
    join ∘ map-local (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 64 ∘
    join ∘ toLocal (map-local (reduce-seq (+) 0)) ∘
    split (blockSize/128) ∘ reorder-stride 128
) ∘ split blockSize
```

```
void reduce6(global float* g idata,
             global float* g odata,
             unsigned int n,
             local volatile float* l data) {
 unsigned int tid = get local id(0);
 unsigned int i =
   get_group_id(0) * (get_local_size(0)*2)
                    + get_local_id(0);
 unsigned int gridSize =
   WG_SIZE * get_num_groups(0);
 l_data[tid] = 0;
 while (i < n) {
   l_data[tid] += g_idata[i];
    if (i + WG SIZE < n)</pre>
      l data[tid] += g idata[i+WG SIZE];
   i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
 if (WG SIZE >= 256) {
    if (tid < 128) {
      l_data[tid] += l_data[tid+128]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
 if (WG_SIZE >= 128) {
    if (tid < 64) {
      l data[tid] += l data[tid+ 64]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
 if (tid < 32) {
    if (WG SIZE >= 64) {
      l_data[tid] += l_data[tid+32]; }
   if (WG_SIZE >= 32) {
      l data[tid] += l data[tid+16]; }
   if (WG SIZE >= 16) {
      l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
      l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) {
      l data[tid] += l data[tid+ 2]; }
    if (WG SIZE >= 2) {
      l_data[tid] += l_data[tid+ 1]; } }
 if (tid == 0)
    g_odata[get_group_id(0)] = l_data[0];
```

# 2 Algorithmic Rewrite Rules

- Provably correct rewrite rules
- Express algorithmic implementation choices

#### Split-join rule:

```
map \ f \rightarrow join \circ map \ (map \ f) \circ split \ n
```

#### Map fusion rule:

```
map \ f \circ map \ g \to map \ (f \circ g)
```

#### Reduce rules:

```
reduce f \ z \to reduce \ f \ z \circ reduce Part \ f \ z

reduce Part \ f \ z \to reduce Part \ f \ z \circ reorder

reduce Part \ f \ z \to join \ \circ map \ (reduce Part \ f \ z) \circ split \ n

reduce Part \ f \ z \to iterate \ n \ (reduce Part \ f \ z)
```



# **2** OpenCL Primitives

#### **Primitive**

**OpenCL concept** 

mapGlobal

Work-items

workgroups global threads

local threads

map Work group

Work-groups

mapLocal

mapSeq

reduceSeq

Sequential implementations

toLocal, toGlobal

Memory areas

map Vec, split Vec, join Vec

**Vectorisation** 



## 2 OpenCL Rewrite Rules

Express low-level implementation and optimisation choices

#### Map rules:

```
map\ f 	o map\ Workgroup\ f \mid map\ Local\ f \mid map\ Global\ f \mid map\ Seq\ f
```

#### Local/ global memory rules:

```
mapLocal\ f \rightarrow toLocal\ (mapLocal\ f) mapLocal\ f \rightarrow toGlobal\ (mapLocal\ f)
```

#### **Vectorisation rule:**

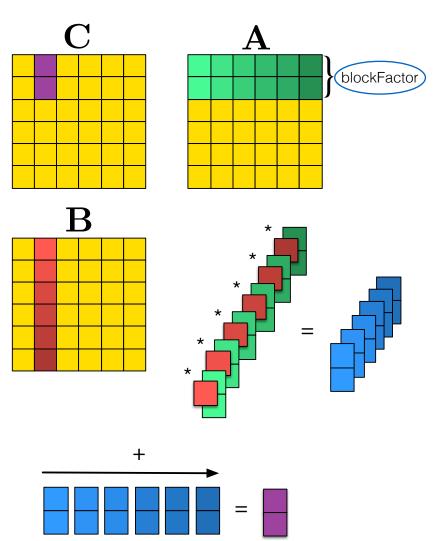
```
map\ f \rightarrow join\ Vec \circ map\ (map\ Vec\ f) \circ split\ Vec\ n
```

#### Fusion rule:

```
reduceSeq\ f\ z\circ mapSeq\ g \rightarrow reduceSeq\ (\lambda\ (acc,x).\ f\ (acc,g\ x))\ z
```



# 2 Optimisation Example: Register Blocking



```
kernel void KERNEL(
 1
 2
      const global float* restrict A,
 3
      const global float* restrict B,
      global float* C, int K, int M, int N)
 5
 6
      float acc blockFactor);
 8
      for (int glb_id_1 = get_global_id(1);
 9
            glb_id_1 < M / blockFactor;
           glb_id_1 += get_global_size(1)) {
10
        for (int glb_id_0 = get_global_id(0); glb_id_0 < N;
11
12
            glb_id_0 += get_global_size(0) {
13
14
          for (int i = 0; i < K; i += 1)
            float temp = B[i * N + glb_id_0];
15
            for (int j = 0; j < blockFactor, <math>j+=1)
16
17
              acc[j] +=
                A[blockFactor * glb_id_1 * K + j * K + i]
18
19
                  * temp;
20
21
          for (int j = 0; j < blockFactor; j += 1)
22
            C[blockFactor * glb_id_1 * N + j * N + glb_id_0]
23
               = acc[j];
24
25
26
```

# 2 Register Blocking as a Macro Rule

- Optimisations are expressed as Macro Rules:
  - Series of Rewrites applied to achieve an optimisation goal

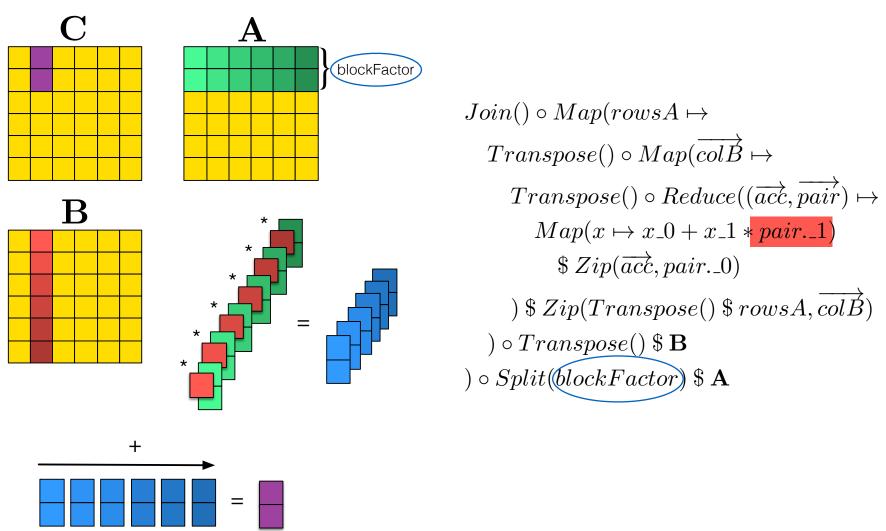
```
registerBlocking = \\ Map(f) \Rightarrow Join() \circ Map(Map(f)) \circ Split(k) \\ Map(a \mapsto Map(b \mapsto f(a,b))) \Rightarrow Transpose() \circ Map(b \mapsto Map(a \mapsto f(a,b))) \\ Map(f \circ g) \Rightarrow Map(f) \circ Map(g) \\ Map(Reduce(f)) \Rightarrow Transpose() \circ Reduce((acc,x) \mapsto Map(f) \circ Zip(acc,x)) \\ Map(Map(f)) \Rightarrow Transpose() \circ Map(Map(f)) \circ Transpose() \\ Transpose() \circ Transpose() \Rightarrow id \\ Reduce(f) \circ Map(g) \Rightarrow Reduce((acc,x) \mapsto f(acc,g(x))) \\ Map(f) \circ Map(g) \Rightarrow Map(f \circ g)
```



# 2 Register Blocking as a Series of Rewrites

```
Join() \circ Map(rowsA \mapsto \\ Map(\overrightarrow{rowA} \mapsto \\ Map(\overrightarrow{colB} \mapsto \\ Reduce(+) \circ Map(*) \\ \$ Zip(\overrightarrow{rowA}, \overrightarrow{colB}) \\) \circ Transpose() \$ \mathbf{B}
) \$ \mathbf{A}
Transpose() \circ Reduce((\overrightarrow{acc}, \overrightarrow{pair}) \mapsto \\ Map(x \mapsto x \cdot 0 + x \cdot 1 * pair \cdot . 1) \\ \$ Zip(\overrightarrow{acc}, pair \cdot . 0) \\ \$ Zip(Transpose() \$ rowsA, \overrightarrow{colB}) \\) \circ Transpose() \$ \mathbf{B} \\) \circ Split(blockFactor) \$ \mathbf{A}
```

# ② Register Blocking Functionally Expressed



### Walkthrough

rewrite rules





```
vecSum = reduce o join o map-workgroup (
    join o toGlobal (map-local (map-seq id)) o split 1 o
    join o map-warp (
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 1 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 2 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 4 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 8 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 16 o
        join o map-lane (reduce-seq (+) 0) o split 2 o reorder-stride 32
        ) o split 64 o
        join o map-local (reduce-seq (+) 0) o split 2 o reorder-stride 64 o
        join o toLocal (map-local (reduce-seq (+) 0)) o
        split (blockSize/128) o reorder-stride 128
        ) o split blockSize
```

```
kernel
void reduce6(global float* g idata,
             global float* g odata,
             unsigned int n,
            local volatile float* l_data) {
 unsigned int tid = get local id(0);
 unsigned int i =
   get_group_id(0) * (get_local_size(0)*2)
                    + get_local_id(0);
 unsigned int gridSize =
   WG SIZE * get num groups(0);
 l_data[tid] = 0;
 while (i < n) {
   l_data[tid] += g_idata[i];
   if (i + WG SIZE < n)</pre>
     l_data[tid] += g_idata[i+WG_SIZE];
   i += gridSize; }
 barrier(CLK_LOCAL_MEM_FENCE);
 if (WG SIZE >= 256) {
   if (tid < 128) {
     l_data[tid] += l_data[tid+128]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
 if (WG_SIZE >= 128) {
   if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
 if (tid < 32) {
   if (WG_SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
   if (WG SIZE >= 32) {
     l data[tid] += l data[tid+16]; }
   if (WG SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
   if (WG SIZE >= 8) {
     l_data[tid] += l_data[tid+ 4]; }
   if (WG SIZE >= 4) {
     l data[tid] += l data[tid+ 2]; }
   if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
 if (tid == 0)
   g_odata[get_group_id(0)] = l_data[0];
```

### Walkthrough

vecSum = reduce (+) 0

rewrite rules code generation



```
join ∘ toGlobal (map-local (map-seq id)) ∘ split 1 ∘
  join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 1 ∘
  join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 2 ∘
  join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 4 ∘
  join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 8 ∘
  join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 16 ∘
  join ∘ map-lane (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 32
) o split 64 o
join ∘ map-local (reduce-seq (+) 0) ∘ split 2 ∘ reorder-stride 64 ∘
split (blockSize/128) o reorder-stride 128
```

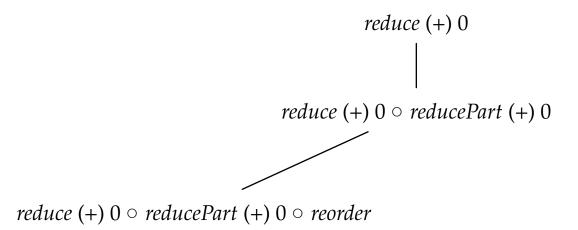
```
kernel
void reduce6(global float* g idata,
             global float* g odata,
             unsigned int n,
            local volatile float* l_data) {
 unsigned int tid = get local id(0);
 unsigned int i =
   get_group_id(0) * (get_local_size(0)*2)
                    + get_local_id(0);
 unsigned int gridSize =
   WG SIZE * get num groups(0);
 l_data[tid] = 0;
 while (i < n) {
   l_data[tid] += g_idata[i];
   if (i + WG SIZE < n)</pre>
     l data[tid] += g idata[i+WG SIZE];
   i += gridSize; }
 barrier(CLK_LOCAL_MEM_FENCE);
 if (WG SIZE >= 256) {
   if (tid < 128) {
     l_data[tid] += l_data[tid+128]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
 if (WG_SIZE >= 128) {
   if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
 if (tid < 32) {
   if (WG_SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
   if (WG SIZE >= 32) {
     l data[tid] += l data[tid+16]; }
   if (WG SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
   if (WG SIZE >= 8) {
     l_data[tid] += l_data[tid+ 4]; }
   if (WG SIZE >= 4) {
     l data[tid] += l data[tid+ 2]; }
   if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
 if (tid == 0)
   g_odata[get_group_id(0)] = l_data[0];
```

## **3 Pattern based OpenCL Code Generation**

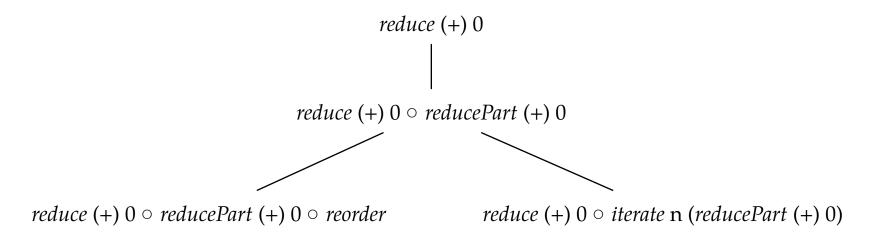
Generate OpenCL code for each OpenCL primitive



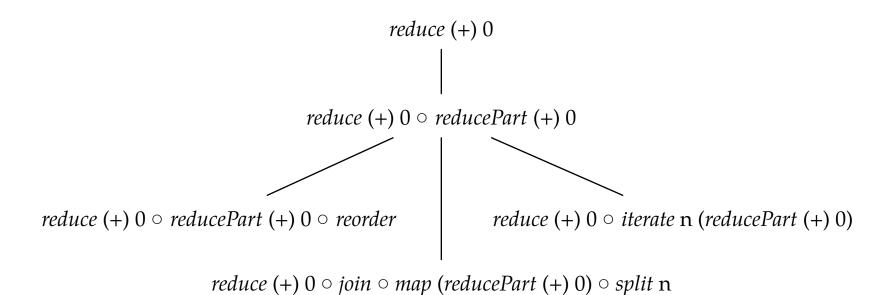




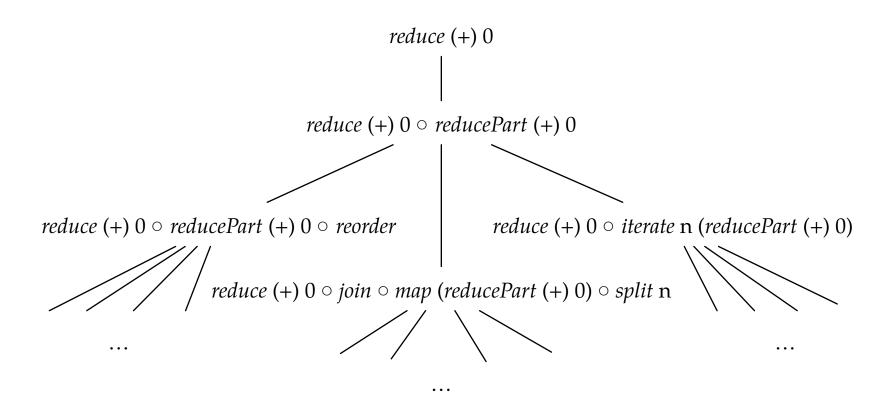


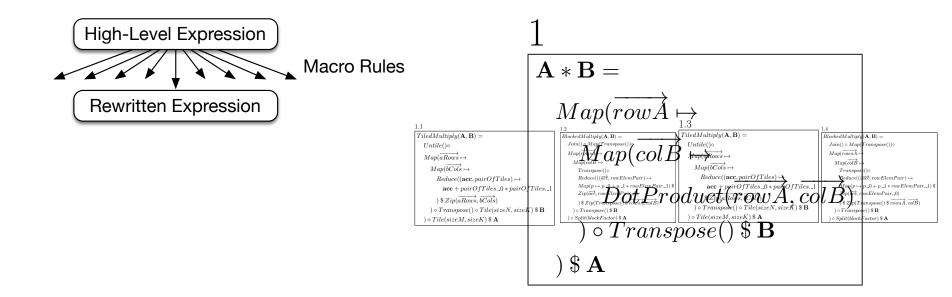




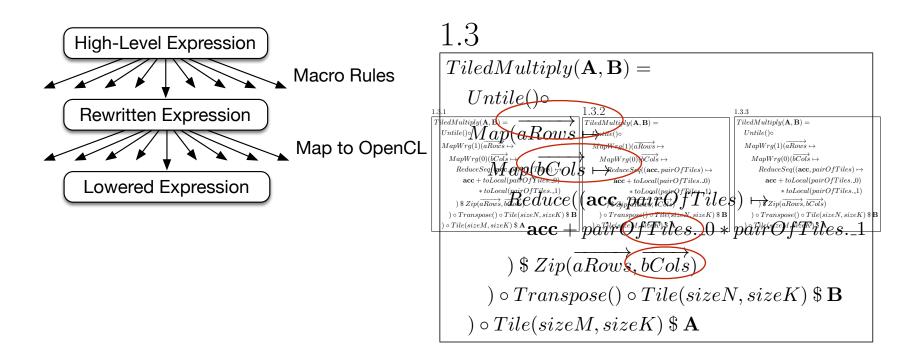




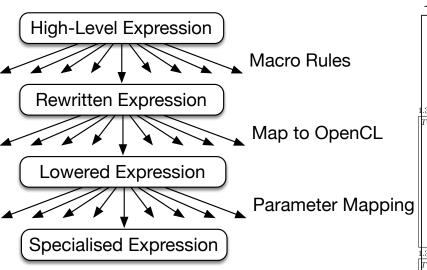




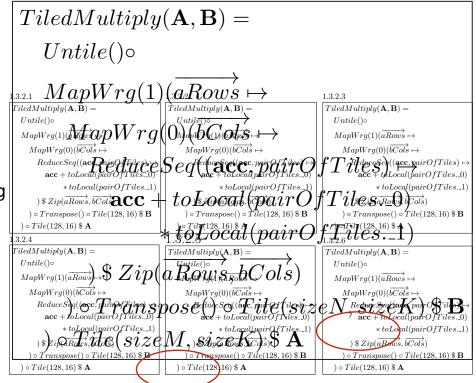




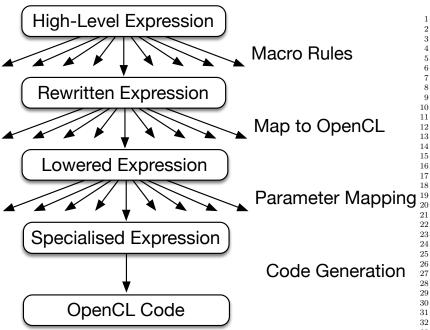




#### 1.3.2







#### 1.3.2.5

```
 \overset{	ext{kernel num_and pt/global float}}{\underset{	ext{local most tileA}}{\overset{	ext{form}}{\text{formulative}}} \overset{	ext{float}}{\underset{	ext{float}}{\overset{	ext{float}}{\text{float}}}} \overset{	ext{float}}{\underset{	ext{float}}{\overset{	ext{float}}{\text{float}}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float}}}} \overset{	ext{float}}{\underset{	ext{float}}{\text{float
private float acq.0; 7 .... acc.31; private float blockOfA.0; ...; blockOfA.7; blockOfA.7;
             \operatorname{acc_0} = 0.00 M \operatorname{col} M \operatorname{col} \operatorname{block} g(0) (bC\overline{ols}) \mapsto
                         \begin{array}{l} {\scriptstyle \text{vstore4(vload4(lid1*M/4+2*i*M+16*w1+lid0,A), 16*lid1+lid0, tileA);}} \\ \scriptstyle \text{vstore4(vload4(lid}Rid+ki*N+16*v1+lid0,B), 16*lid1*lid0, tileA);} \\ \scriptstyle \text{barrier } (...) ; \\ ReduceSeq((acc, pair)) \\ \end{array} \mapsto
                             for (int j=0; j<8; j++) { blockOfA_0 = tileA[0+g)+[0+8]+...t blockOfB_0 = tileA[0+g)+[0+8]+...t blockOfB_0 = tileA[0+6+8]+lido]; fTiles._0)
                                  acc_0 += blockOfA_0 * blockOfB_0; ...; acc_3 += blockOfA_7 * blockOfB_3; f = blockOfA_0 * blockOfB_1 * to 19.00000 * blockOfB_0 * blockOfB_0 * blockOfB_0 * blockOfB_2; ...; acc_3 += blockOfA_7 * blockOfB_2; Tiles_1
                                                                                                                                                                                      ) \$ Zip(aRows, bCols)
                \begin{array}{l} C[\ 0+8* \mathrm{lid} 1*N+64* w0+64* w1*N+0*N+\mathrm{lid} 0] = \mathrm{acc}\ 0, \dots; C[\ 0+8* \mathrm{lid} 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 2.8; \\ C[\ 16+8* \mathrm{lid} 1*N+64* w0+64* w1*N+0*N+\mathrm{lid} 0] = \mathrm{acc}\ 2.\dots; C[\ 32+8* \mathrm{lid} 1*N+64* w0+64* w1*N+0*N+\mathrm{lid} 0] = \mathrm{acc}\ 2.\dots; C[\ 32+8* \mathrm{lid} 1*N+64* w0+64* w1*N+0*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.0; \\ C[\ 48+8* \mathrm{lid} 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid} 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid} 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid} 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid} 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid} 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid} 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid} 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid} 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid} 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid} 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid}\ 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid}\ 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid}\ 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid}\ 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid}\ 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid}\ 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid}\ 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid}\ 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid}\ 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid}\ 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid}\ 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid}\ 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid}\ 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}\ 3.1; \\ C[\ 48+8* \mathrm{lid}\ 1*N+64* w0+64* w1*N+7*N+\mathrm{lid} 0] = \mathrm{acc}
                                                                                                    \circ Tile(128, 16) \$ A
```



## **Heuristics for Matrix Multiplication**

#### For Macro Rules:

- Nesting depth
- Distance of addition and multiplication
- Number of times rules are applied

#### For Map to OpenCL:

- Fixed parallelism mapping
- Limited choices for mapping to local and global memory
- Follows best practice

#### For Parameter Mapping:

- Amount of memory used
  - Global
  - Local
  - Registers
- Amount of parallelism
  - Work-items
  - Workgroup

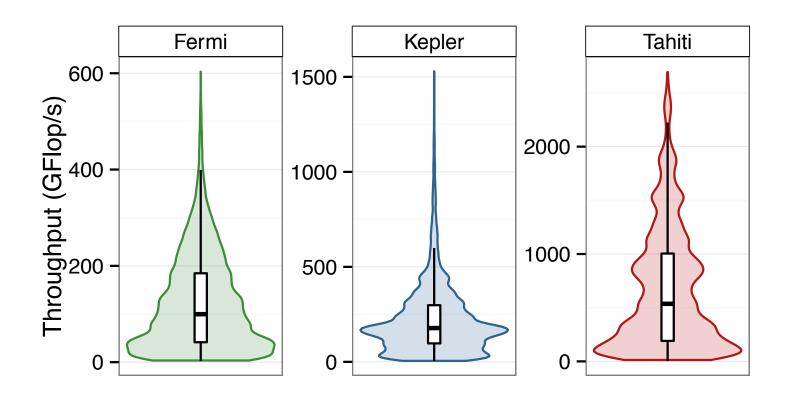


# Exploration in Numbers for Matrix Multiplication

#### Program Variants: Phases: High-Level Program 1 Algorithmic **Exploration** Algorithmic 8 Rewritten Program OpenCL specific **Exploration** OpenCL Specific 760 Program Parameter **Exploration Fully Specialized** 46,000 Program Code Generation OpenCL Code 46,000



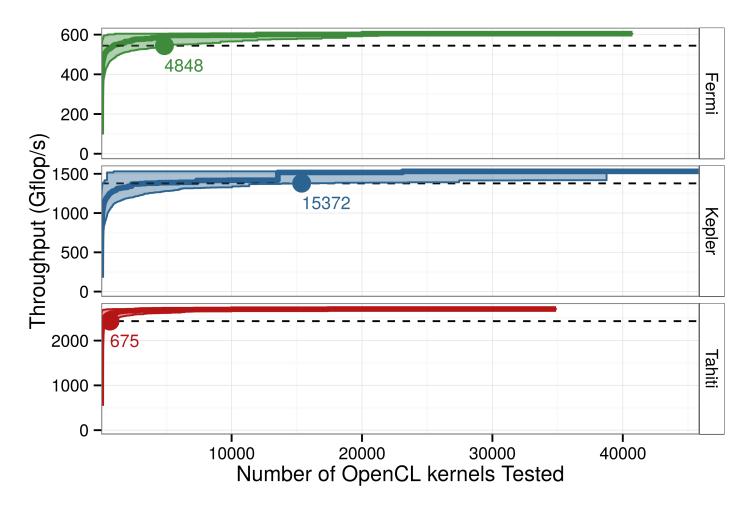
## **Exploration Space for Matrix Multiplication**



Only few OpenCL kernel with very good performance



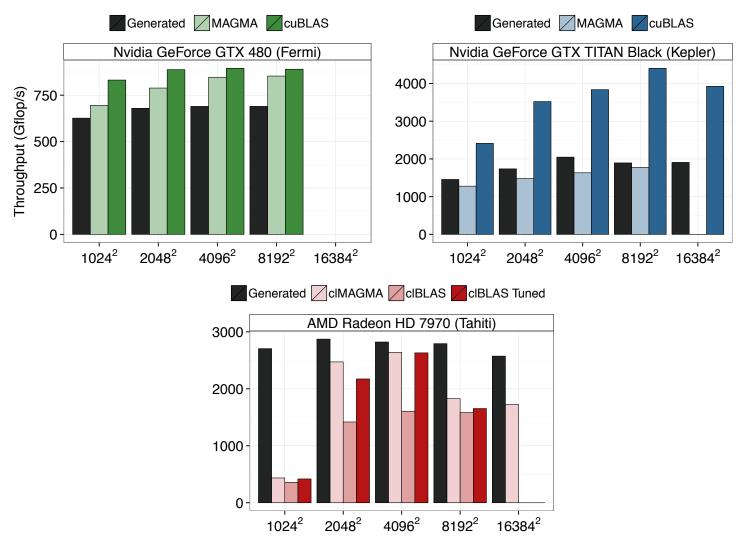
#### **Performance Evolution for Randomised Search**



Even with a simple random search strategy one can expect to find a good performing kernel quickly



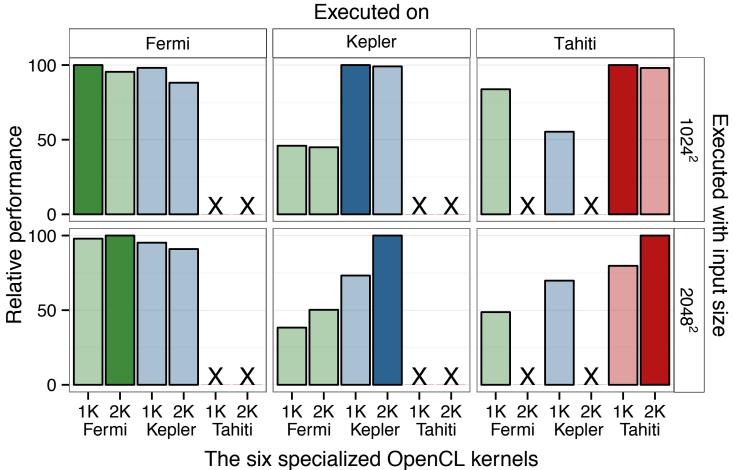
## **Performance Results Matrix Multiplication**



Performance close or better than hand-tuned MAGMA library



## **Performance Portability Matrix Multiplication**



Generated kernels are specialised for device and input size



#### **Summary**

- OpenCL code is hard to write and not performance portable
- Our approach uses
  - portable and functional high-level primitives,
  - OpenCL-specific low-level primitives, and
  - rewrite-rules to generate high performance code.
- Rewrite-rules define a space of possible implementations
- Performance on par with specialised, highly-tuned code



Michel Steuwer michel.steuwer@ed.ac.uk



Thibaut Lutz
Now with Nyidia



Toomas Remmelg toomas.remmelg@ed.ac.uk

More details in the ICFP 2015, GPGPU 2016, CASES 2016 papers available at:

http://www.lift-project.org

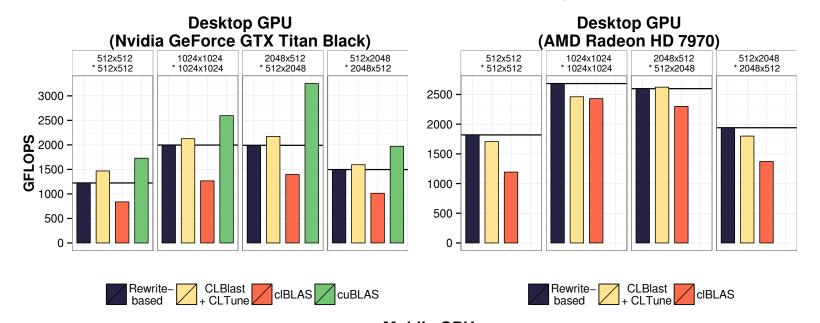


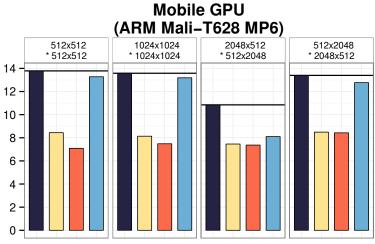
supported by:



Oracle Labs

### **More Results Matrix Multiplication**



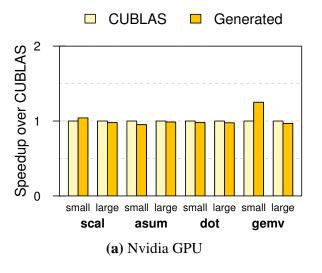


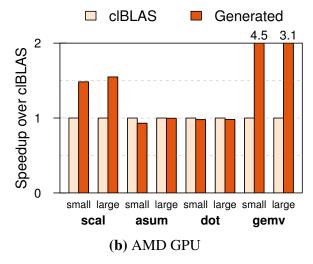


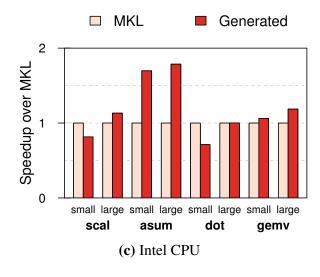


#### **Performance Results more Benchmarks**

#### vs. Hardware-Specific Implementations





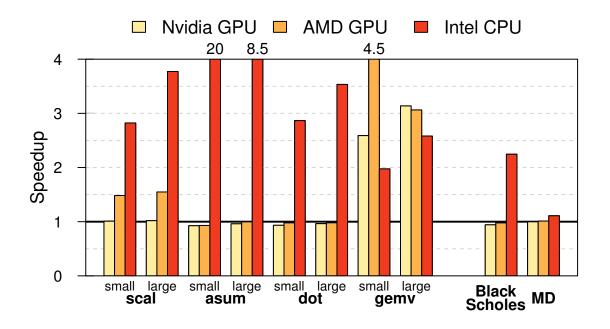


- Automatically generated code vs. expert written code
- Competitive performance vs. highly optimised implementations
- Up to **4.5x** speedup for *gemv* on AMD



#### **Performance Results more Benchmarks**

vs. Portable Implementation



• Up to **20x** speedup on fairly simple benchmarks vs. portable clBLAS implementation

